Intro to GoWin FPGA's with built in microprocessors

June 2021

Les MacInnes – FAE Redtree Solutions

Agenda

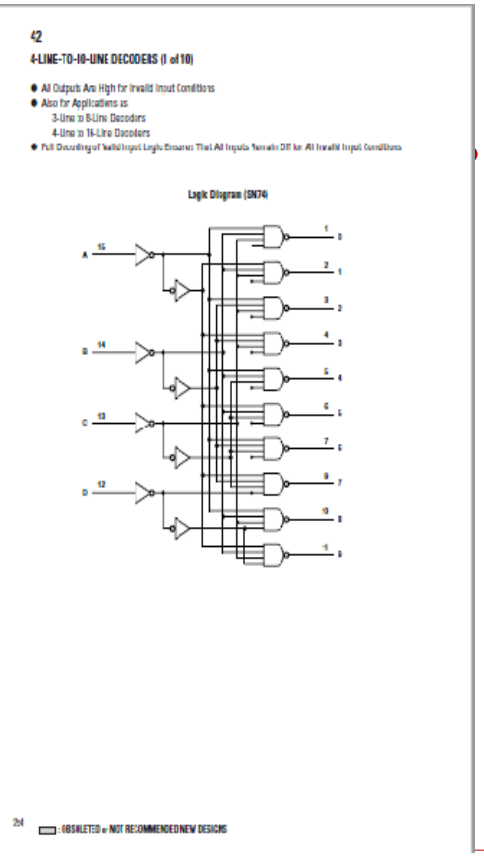
- Beginners guide to Programmable logic
  - Simplified explanation of FPGA's\CPLD's and their evolution
  - Design entry methods
  - Simplified explanation of FPGA design tool flow
- GoWin
  - Product line up
  - Hard and soft microprocessor core options
  - Architecture of hard M3 on GW1NS
  - Overview of the tools
  - Typical applications
  - Q and A

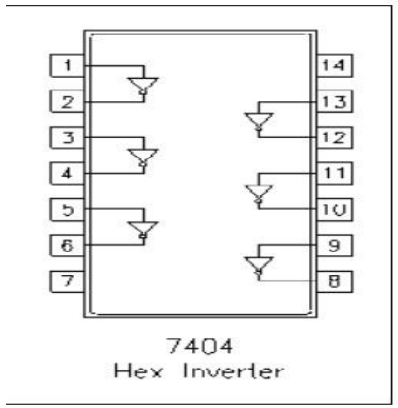
What is Programmable Logic?

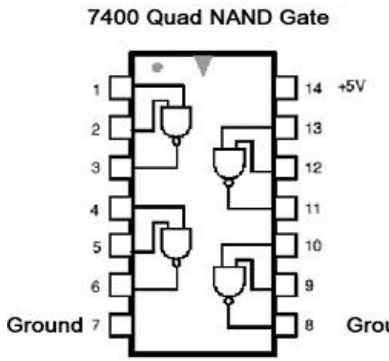
- You could say originally every electronic system had three basic types of digital devices: memory, microprocessors and logic
- Memory devices stored information such as the code to configure a system or the data being used in the system
- Microprocessors executed software instructions that performed a wide variety of tasks to run the system program
- Logic devices provided most of the other functions a system needed such as timing and control logic, interfacing, data communication, signal processing, decoder logic and many others.

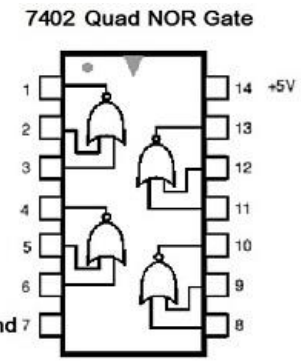
What is Programmable Logic contd

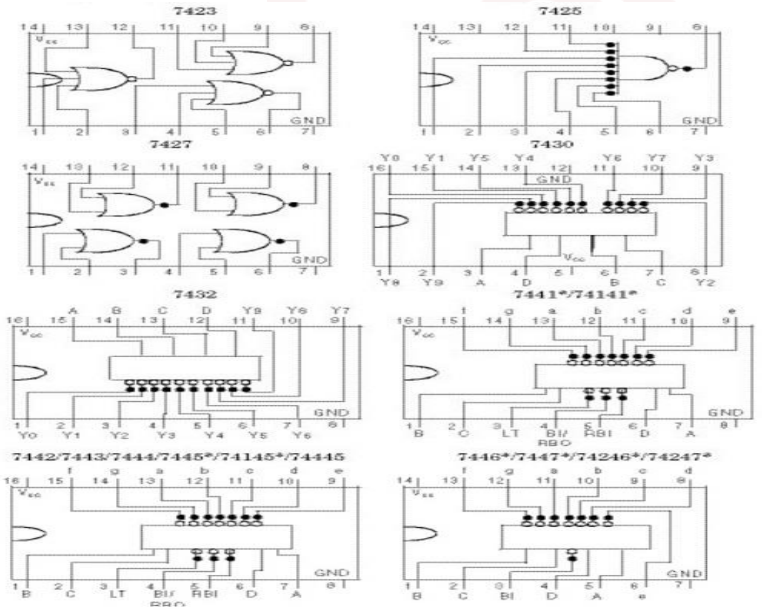
- Logic devices can broadly be classified into two categories – discrete or fixed and programmable
- Discrete logic devices perform one function or set of functions as manufactured. If the customers design changes or needs re-work then the device and probably the PCB layout will need to be changed, incurring significant costs and time.
- Programmable logic devices are still standard off the shelf products but offer the customer a wide range of logic capacity, features and speed which the customer can program and reprogram many times without changing the device











Programmable Logic – lots of acronyms

- PLD – Programmable Logic Device
  - Includes PALs, GALs, SPLDs, CPLDs and FPGAs
- PAL – Programmable Array Logic and GAL – Generic Array Logic
  - PALs and GALs were the smallest programmable logic devices also known as SPLDs (Simple Programmable Logic Devices). - Virtually obsolete.
- CPLD – Complex Programmable Logic Device
  - Usually EE or flash technology with logic densities up to the equivalent of 10K gates\32 or more macrocells. - Have some niche apps.
- FPGA – Field Programmable Gate Arrays
  - Usually SRAM based with gate counts from 50K to multi millions. - Still going strong.
- Gate count refers to a 2 input NAND gate. Meaningless with current devices. Some vendors now state how many billion transistors are in their FPGA.

- These acronyms meant something in the day. Some of them still persist.

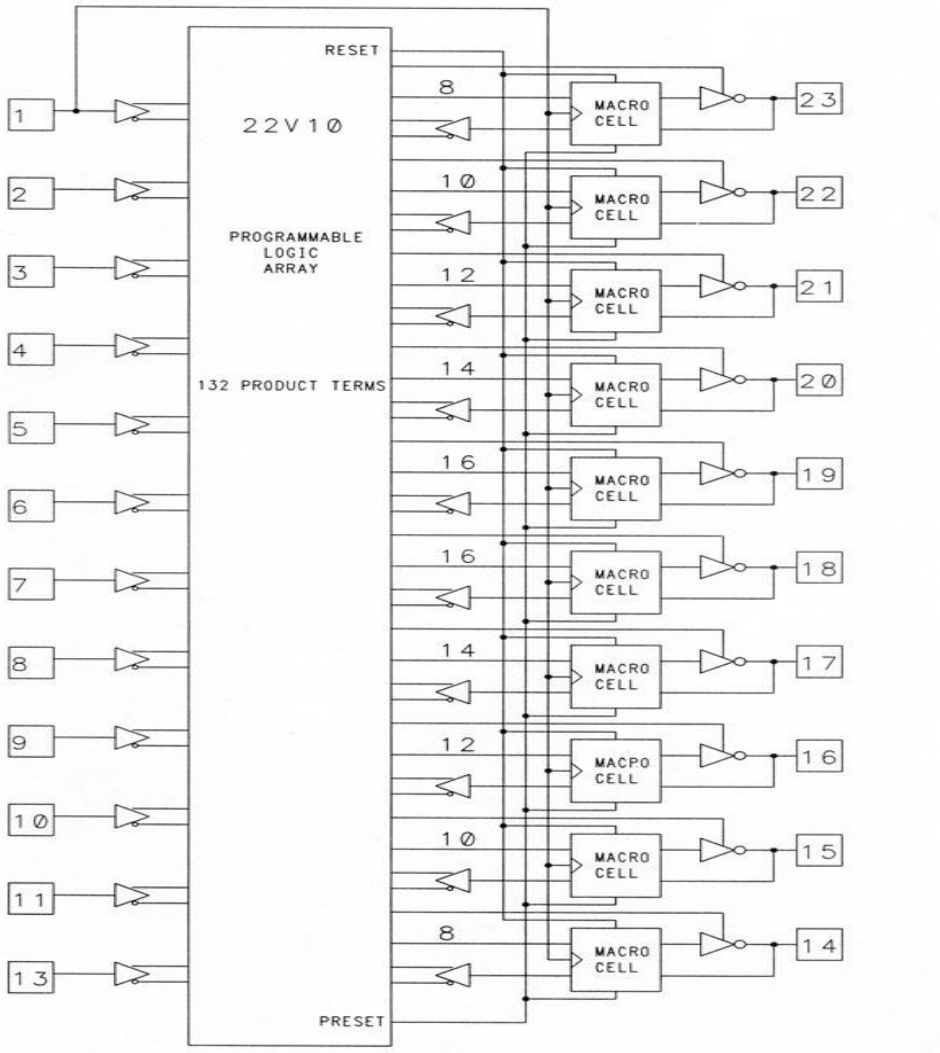
CPLD’s

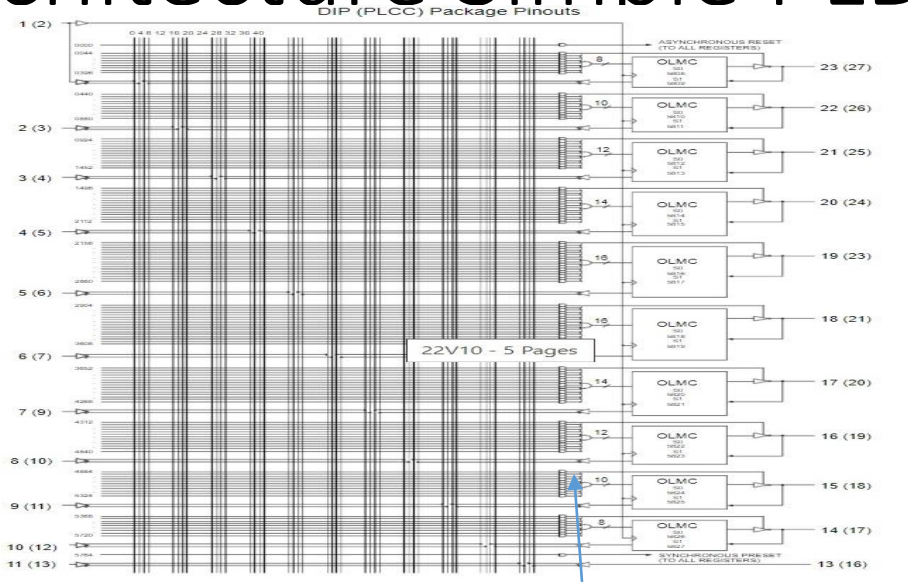
- Macrocell/sum of products (SOP) based
- Usually none volatile Technology
- “Instant ON” Capability
- Originally higher tpd Performance
- More Predictable Timing
- More Efficient Implementation of Wide Functions

FPGA's

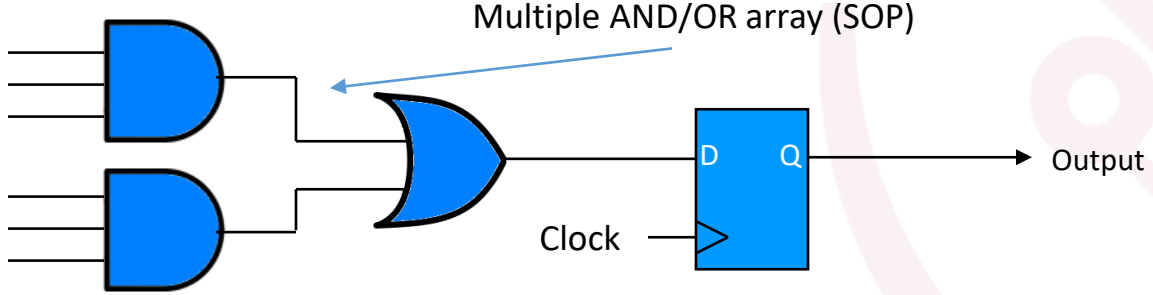
- Originally SRAM based
- Therefore needed an external "boot up"
- Not Instant on
- Supports memory and logic
- Many more registers than CPLDs
- Originally routing through the FPGA could create long timing path delays
- Much higher densities
- Much more IP available due to size
- Has led to System on Chip approach (SOC)
- Much lower cost per LUT compared to a macrocell
- The SRAM based FPGA's tend to migrate relatively easily to the latest technology process node with big increases in performance. The big 2 vendors tend to concentrate on this sector now.

PAL architecture Simple PLD (SPLD)





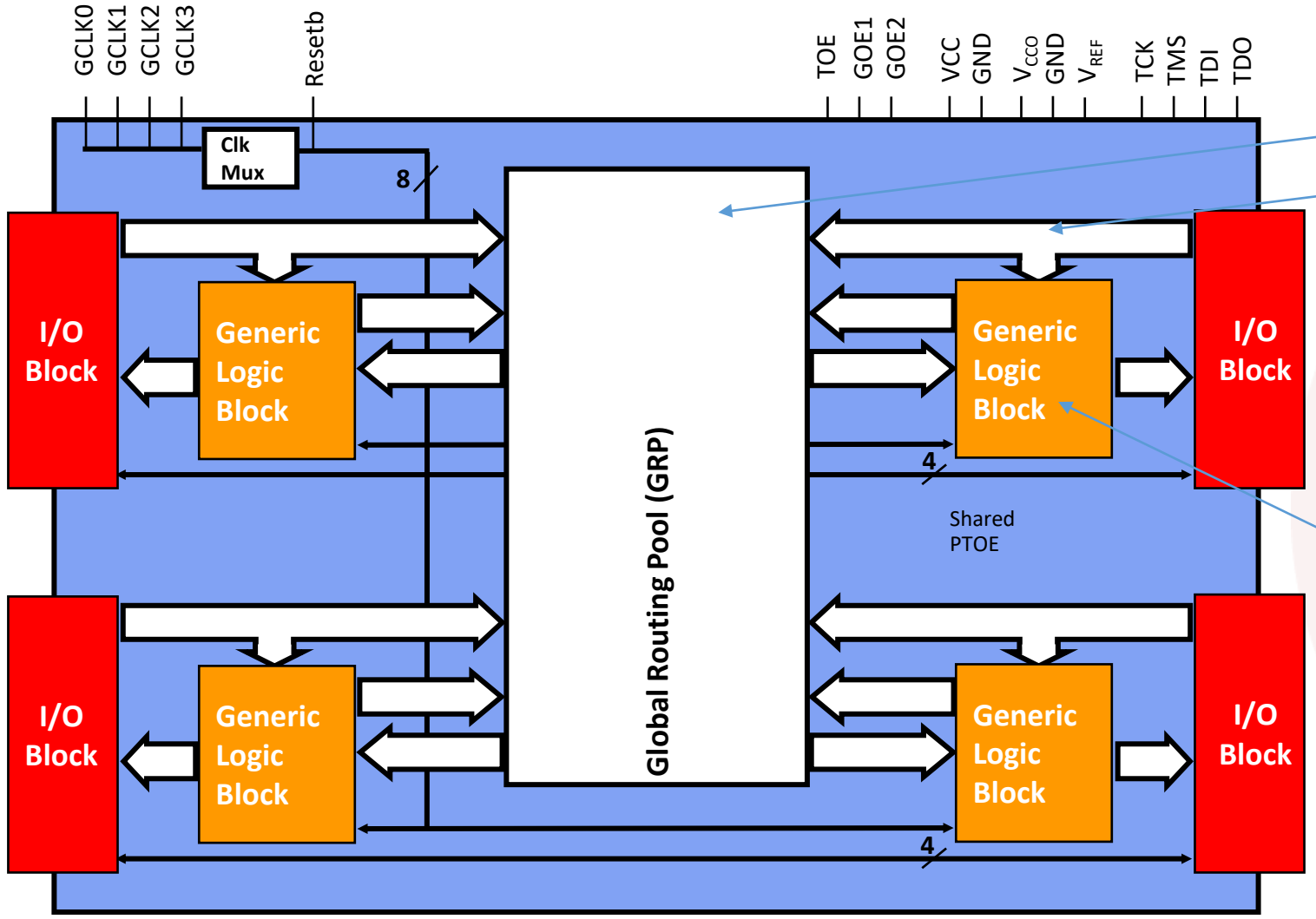
Multiple AND/OR array (SOP)



CPLD's are more or less based on this same building block. With a few more strategic placed bits of hard logic, more flexible IO and a lot bigger.

16L8
16H8
20R10

CPLD block diagram

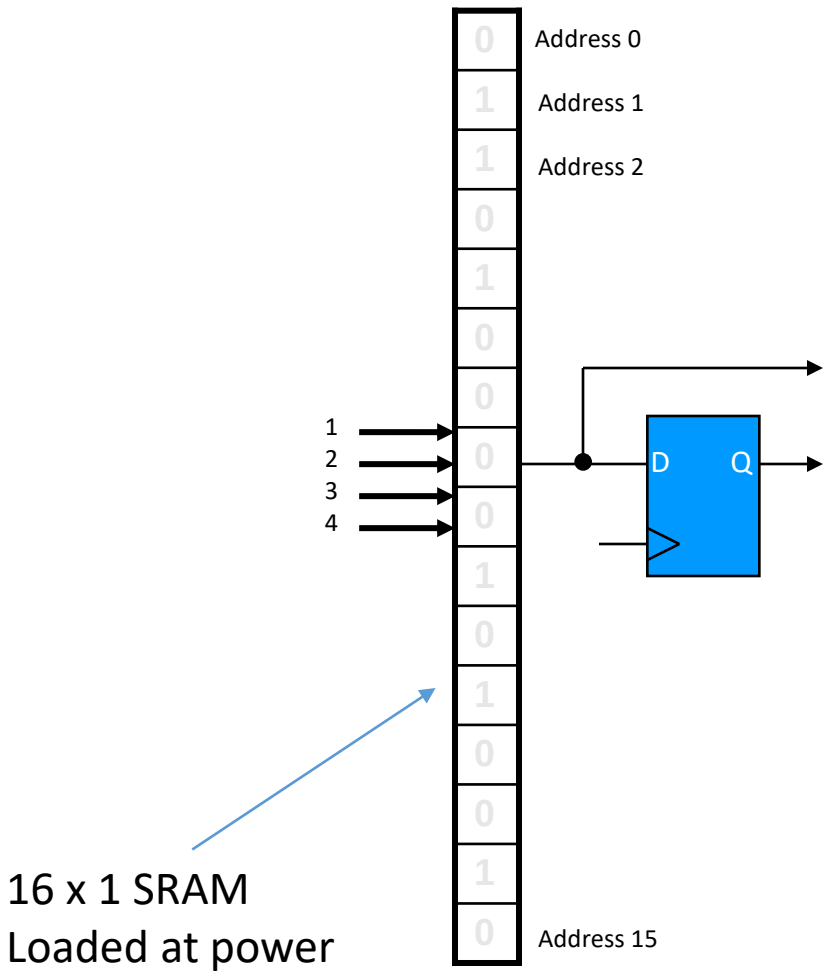


Due to the fixed routing delays it was much easier to get a better estimate of the max operating speed

Huge routing resource with fixed delay regardless of which pins go in and out

Multiple bigger versions of previous slide

Original FPGA basic logic building block



16 x 1 SRAM
Loaded at power up

1	2	3	4	Q
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

4 inputs produce 16 addresses, each address is a bit that stores a user state. Effectively any function of the 4 inputs.
The output cell feeds into a flip flop, we have a building block that can implement a synchronous, or combinatorial function

This is called a 4 input Look Up Table Or 4 input LUT

Some vendors now use 6 input LUT's (64 bit)

XC2064 FPGA

What is not shown here are the switching matrices dotted all over the die to route signals around the device

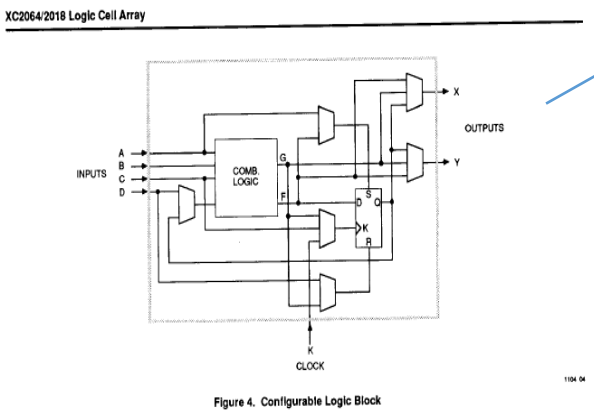


Figure 4. Configurable Logic Block

Figure 8b. XC2064 Long Lines, I/O Clocks, I/O Direct Interconnect

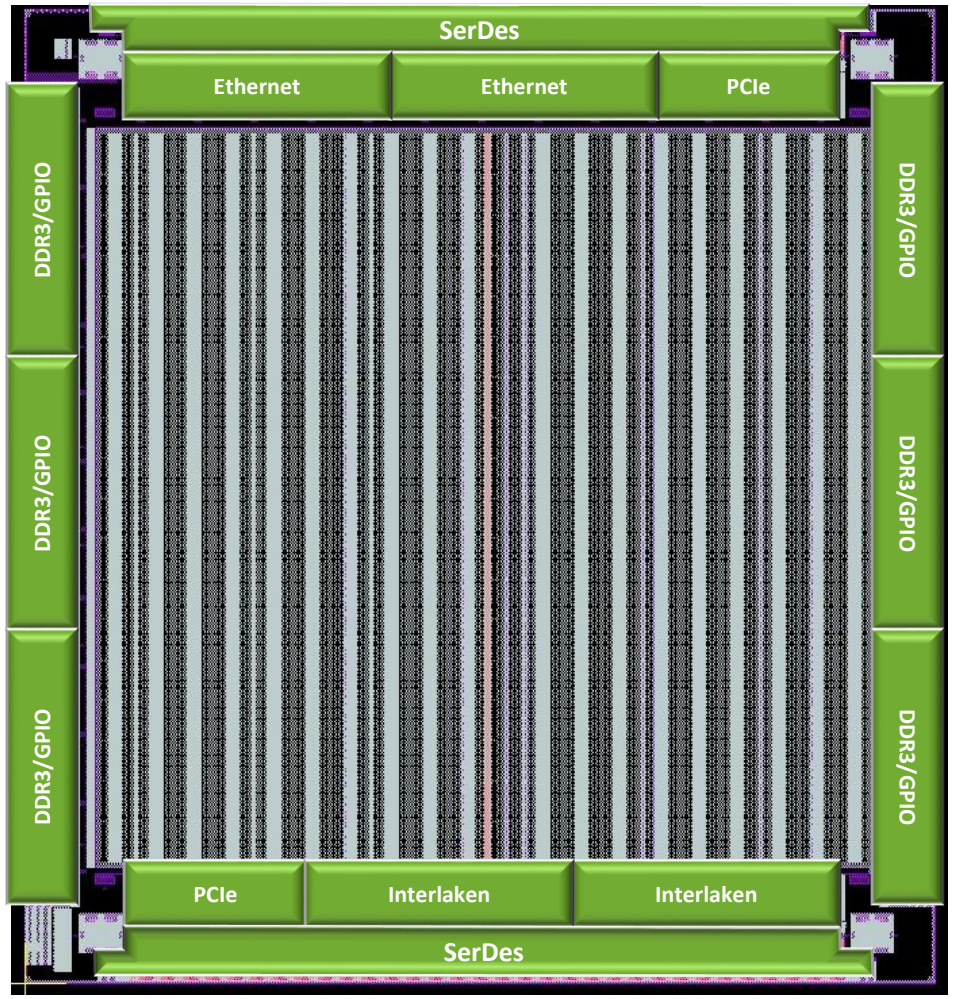
FPGA basics

- Xilinx invented them in the early 1980's – 2000 series. They were also known as LCA's.
- Original devices were based on a 4 input LUT (look up table) structure for part of the programmable portion of the FPGA. The output could be any function of the 4 inputs. The other programmable portion was switching matrices to route signals around the chip. Also each LUT output could be routed to a F-F (flip flop).
- LUT's were SRAM based and had to be loaded from external memory from power up. Each 4 I/P LUT used 16 bits of SRAM. You could also construct small memories using LUT's instead of as logic. This was referred to as distributed memory. This still exists alongside hardened block SRAM.
- The original family had a max of 100 LUT's. This is still used today as a rough guide to the size of the device, though a bit meaningless with all the extra features in them.

FPGA evolution and key features

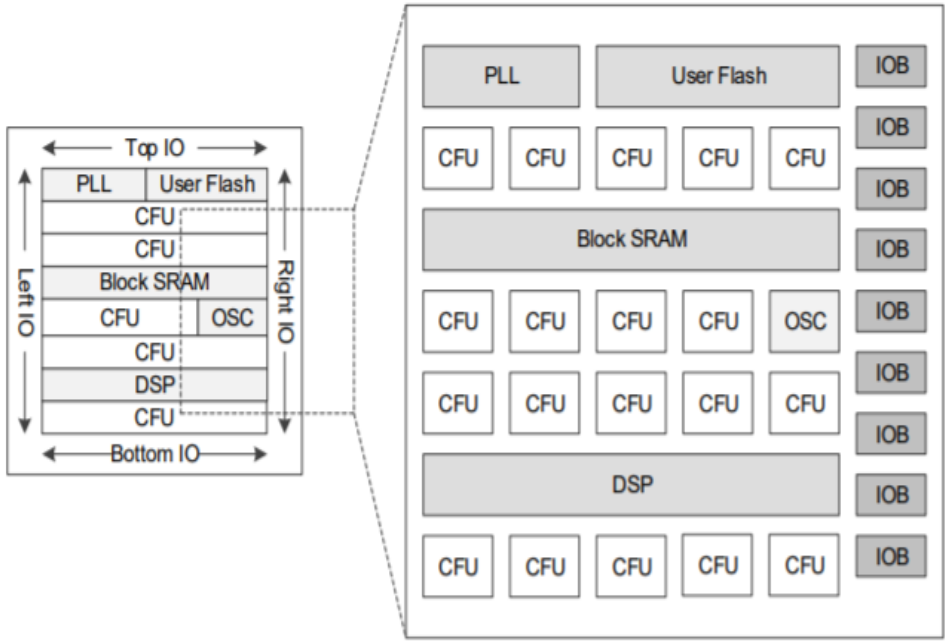
- Newer FPGA's are still based on the same LUT structure, but with lots more features. Such as Embedded hard memories, DSP, PLL's, DLL's, Hardened peripheral interfaces, SERDES, Hardened processors, Hardened external memory interfaces, multiple IO standards, etc, etc. All still with a chunk of LUT's to do some programmable function.
- The architectures of the highest end devices is changing significantly due to going after the AI and data centre accelerators applications. The low and mid range devices still broadly stick to the evolution described.
- The FPGA fabric still needs to be loaded from power up. A number of FPGA vendors have brought out devices that have the configuration memory for this within the FPGA itself. So you program the Flash/E2 with your specific design, then each time it powers up it first loads the config memory from Flash/E2 into the SRAM. This is a key advantage for the GoWin Little Bee family.
- Programming. Originally each vendor had their own proprietary programming interface. This was for either a micro doing the loading, or a PROM. This evolved into JTAG programming including the TAP controller for doing PCB continuity test. You can now program via SPI, or I2C.
- Other key features of FPGA's are speed (Fmax), power consumption, number of IO, package size, migration options within a certain package, design software required, soft IP available, etc, etc.
- A lot of the options are normally in the shortform. Different vendors often use different acronyms for the same basic building blocks.
- Approx 10 years ago the patents for LUT's and the routing\switching matrices ran out. So new FPGA vendors have emerged, including GoWin.

Large FPGA – approx 1 million LUT's



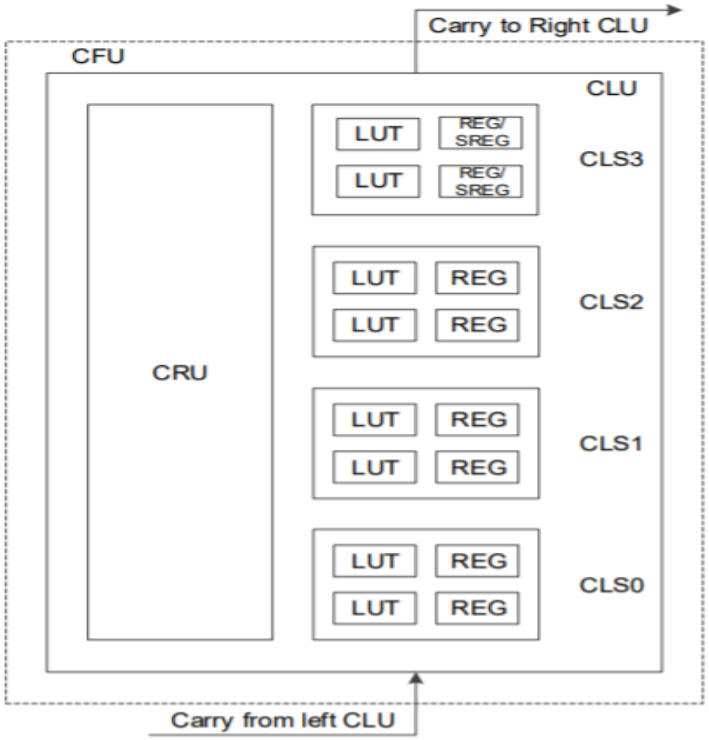
Reference [GW1N Series FPGA Data Sheet DS100]

GW1N Architecture Overview



CFU	Configurable Function Unit
IOB	Input Output Block

CFU Configurable Function Unit



CLU	Configurable Logic Unit
CRU	Configurable Routing Unit
CLS	Configurable Logic Slice
LUT	Look Up Table

HDL design entry

Originally the design entry method was via schematic and/or HDL's. They often came with libraries that allowed you to do designs similar to using 74 series components. The early HDL's were different from one vendor to the next.

There are now 2 main design entry methods. Verilog\System Verilog and VHDL.

VHDL took a number of constructs from ADA. Is more academic and complex than Verilog. Originally came out of a US DOD sponsored program as a way of documenting the behaviour of high speed digital ASIC's used in defence programmes. This evolved into VHDL simulators and then synthesis tools to turn the VHDL code into a physical implementation of the circuit. It became an IEEE standard in 1987. Sometimes can appear over the top for simple designs, but allows easier design of more complex circuits.

Verilog is similar to C. Was originally a commercial simulation product (now owned by Cadence) that was transferred to the public domain to become a standardisation after the release of VHDL. It became an IEEE Standard in 1995.

S/W engineers tend to pick up the syntax quickly. The main difference with software is that in the HDL all the processes/module/entity architecture pair. Are executing concurrently, rather than the sequential nature of a micro.

For both there are lots of free code examples and reference designs.

There have been updates on the original 1987/1995 releases. Most synthesis vendors now allow both languages to be mixed.

Verilog

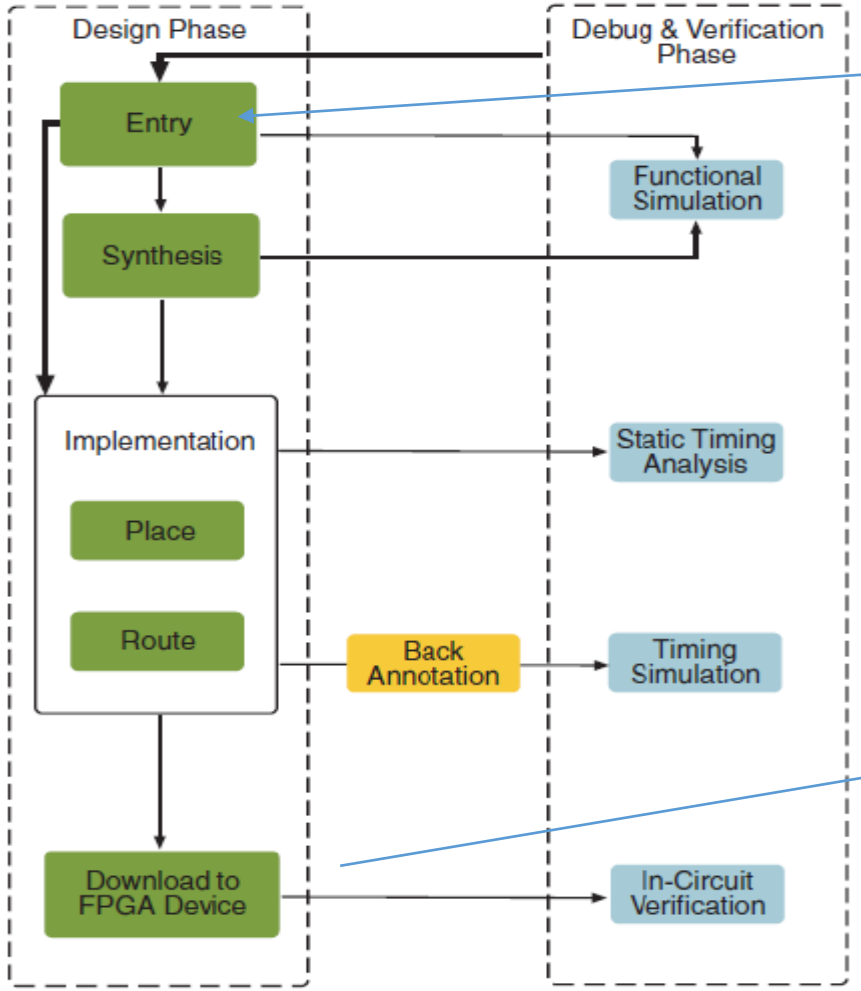
```
// Verilog code for AND-OR-INVERT gate
module AOI (input A, B, C, D, output F);
  assign F = ~((A & B) | (C & D));
endmodule
// end of Verilog code
```

VHDL

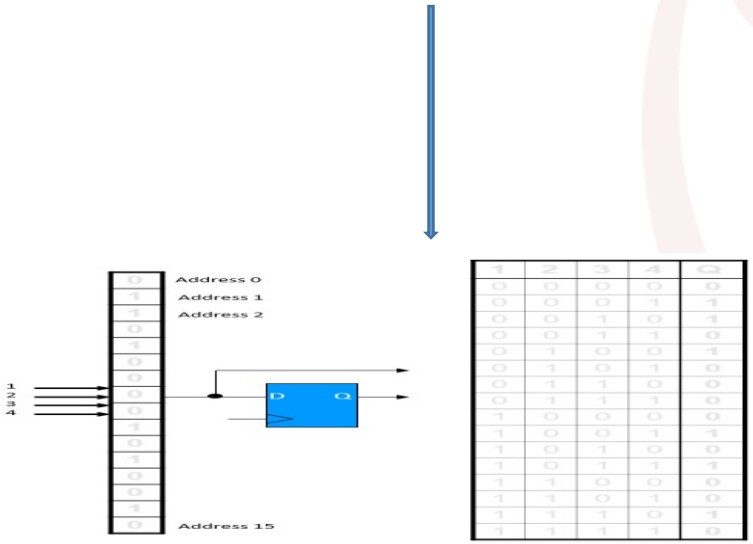
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
 entity AOI is
port (
  A, B, C, D: in STD_LOGIC;
  F : out STD_LOGIC);
end AOI;
 architecture V1 of AOI is
begin
  F <= not ((A and B) or (C and D));
end V1;
-- end of VHDL code
```

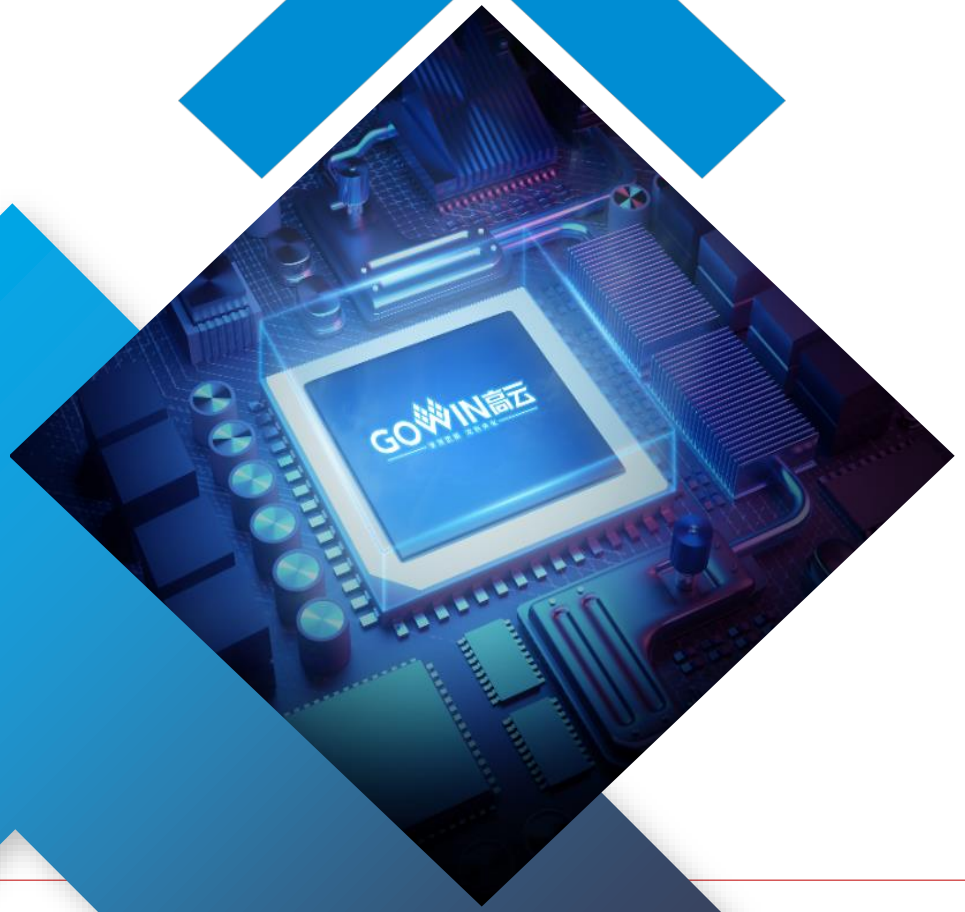
Simplified FPGA design flow through vendor tool chain

Optional




```
// Verilog code for AND-OR-INVERT
gate

module AOI (input A, B, C, D, output F);

  assign F = ~((A & B) | (C & D));

endmodule

// end of Verilog code
```





Introduction to GoWin and the product line up

GOWIN Company Overview

Providing easy to use, high performance, low-cost FPGA solutions for consumer, industrial, automotive, and communications applications.

Locations: Guangdong, China (Corp HQ)
San Jose, California (US HQ)
Hong Kong (Asia HQ)
Shandong, Shanghai, Shenzhen

Manufacturing: Scalable manufacturing capabilities with world-class partners.

Founded: 2014 **Silicon:** 2016 **First revenues:** 2017

World's fastest growing FPGA Company

FPGA Devices: Flash and SRAM Based

Low-Density / Low Power *(LUTs < 10K): GW1N, GW1NR, GW1NS, GW1NRF*

Mid-Density *(10K < LUTs < 100K): GW2A, GW2AR, GW2ANR*

High-Density *(LUTs > 100K): GW5AT, GW4ST*

Key Partners

tsmc, HLMC, HUA TIAN, ASE GROUP, SMIC, arm, mipi alliance, RISC-V

Awards and Recognition

China Annual Creativity in Electronics

ACE AWARDS EE Times EDN

2018

EE Times Silicon 60

2015 & 2016

Most Remarkable Global Technology Startup

GOWIN FPGA Families

Flash Based FPGAs
1-10K Logic Element Density

Consumer, Mobile and IoT

- As small as 1.8 x 1.8mm
- Interface Bridging and Multiplexing

Industrial, Commercial and Server

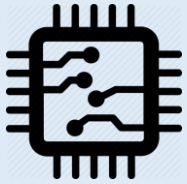
- TQFP, QFN and BGA (0.8mm) Packaging
- CPLD Replacement, Power/Platform Management

SRAM Based FPGAs
20-55K Logic Element Density

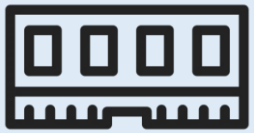
Communications, Industrial and Automotive

- As small as 8x8mm
- Up to 607 user interface pins
- 1.2 Gbps LVDS, DDR3, MIPI D-PHY, PCI
- High Speed Interfacing and IO Expansion

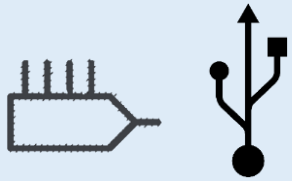
Differentiating FPGA Features



Hardened MCUs
Arm Cortex-M3



On-Chip Memory
Up to 16MB



More Interfaces
ADC, USB, SPMI, I3C

Ultra-Low Power
10µW Sleep

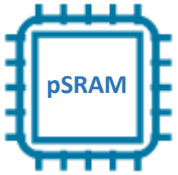
Security
PUF Based RoT

GOWIN FPGA Product Families

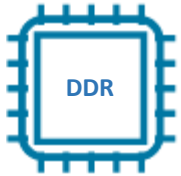
		GOWIN *FPGA* Family Devices			
		LittleBee Flash-Based FPGA **GW1N*** 1-10K Logic Element Density			Arora SRAM-Based FPGA **GW2A*** 20-55K Logic Element Density
Product Features	**Ultra-Low Power** SPMI Power Management	***Z**			
	Hard MCU ARM Cortex-M3 ARC EM4	***S**	***SR**		
	Extended Memory On-Chip SRAM	***R**			***R**
	Security SRAM PUF Root-of-Trust			***SE** ***SER**	
	Bluetooth Low Energy RF Transceiver	***RF**			
	Arora plus Flash				***N**
	Arora plus SRAM & Flash				***NR**

Product Series	Density (LUTs)	LittleBee	Arora
GW1N	1K, 2K, 4K, 9K	Flash-Based FPGA	N/A
GW1NZ	1K	Ultra-Low Power	
GW1NS	2K, 4K	Embedded Hardcore MCU	
GW1NR	1K, 4K, 9K	Extended Memory	
GW1NSR	2K, 4K	MCU + Memory	
GW1NSE	2K, 4K	MCU + Security	
GW1NSER	2K. 4K	MCU + Security + Memory	
GW1NRF	4K	MCU + Security + RF Transceiver	
GW2A	20K, 55K	N/A	RAM-Based FPGA
GW2AR	20K		On-Chip Memory
GW2AN	20K		On-Chip NOR Flash
GW2ANR	20K		On-Chip Memory Plus, NOR Flash

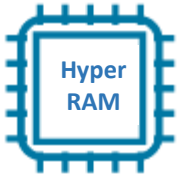
GOWIN FPGA On-Chip Memory Options



128Mbits DDR
- Data Width: 16-bits
- Clock Freq: 166MHz

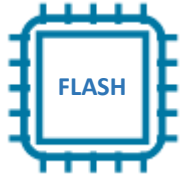


128Mbits DDR
- Data Width: 16-bits
- Clock Freq: 200MHz



64Mbits DDR
- Data Width: 8-bits
- Clock Freq: 200MHz

64Mbits SDR
- Data Width: 32-bits
- Clock Freq: 166MHz



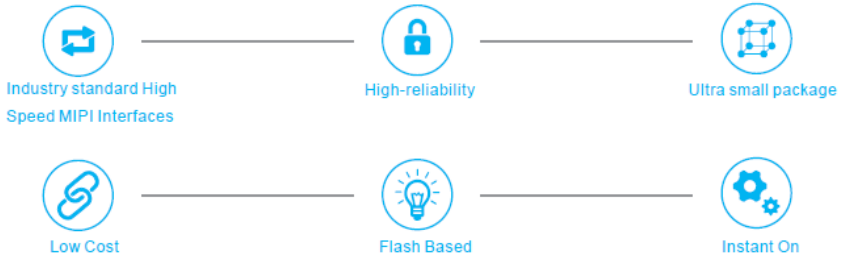
32Mbits SDR
- Data Width: 1-bit
- Clock Freq: 120MHz

GOWIN FPGA Embedded Memory Options					
Device	**Memory Technology**	**Capacity (MBytes)**	**Clock (MHz)**	**Data Width (Bits)**	**Comments**
GW1NR	NOR Flash (FN32G)	4	100	1	Additional on-chip FLASH Memory
	SDR SDRAM	8	Up to 200	16	Max Clock Speed depends on package.
	DDR pSRAM	Up to 16	166 (equivalent DDR332)	16 32 (MG100)	Memory Capacity depends on package.
GW1NSR-4C	NOR Flash (QN48G)	4	120	1	Flash Memory supports additional ARM instruction code.
	DDR HyperRAM (QN48P)	Up to 8	200 (equivalent DDR400)	8	Hardcore ARM Cortex M3 Memory Capacity depends upon memory technology & package.
GW1NSR–2/2C	DDR pSRAM	Up to 4	166 (equivalent DDR332)	8	Max Capacity depends upon memory technology & package.
GW1NSR–4/4C	DDR pSRAM	Up to 8	166 (equivalent DDR332)	16	Max Capacity depends upon memory technology & package.
GW2AR	SDR SDRAM	8	166	32	
	DDR SDRAM	16	200/250	16	Max Clock Speed depends on package.
	DDR pSRAM	8	166 (equivalent DDR332)	16	
GW2ANR	SDR SDRAM	8	166	32	
	NOR Flash	4	120	1	Flash Memory

LittleBee GW1N (Base Family)

Flash-Based, Non-Volatile, Instant On, Low Power, Low Cost, Small Package Options

Resource	GW1N-1	GW1N-2 Available Q1-2021	GW1N-4	GW1N-9
LUT4	1152	2304	4608	8640
Flip-Flop	864	2304	3456	6480
Shadow S-SRAM (Bits)	-	-	-	17280
Block B-SRAM (bits)	72K	72K	180K	468K
B-SRAM Blocks	4	4	10	26
User Flash (Bits)	96K	256K	256K	608K
Mult 18x18	-	-	16	20
PLLs	1	1	2	2
I/O Banks	4	6	4	4
Max I/O	120	126	218	276
Core Voltage ZV	-	0.9V	-	-
Core Voltage LV	1.2V	1.2V	1.2V	1.2V
Core Voltage UV	1.8V/2.5V/3.3V Only LQ100X	1.8V/2.5V/3.3V	2.5V/3.3V	2.5V/3.3V

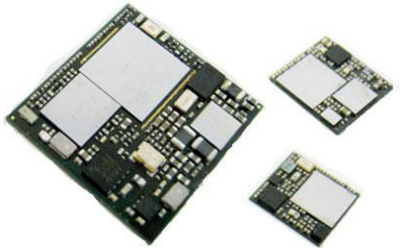


Package	Pitch(mm)	Size(mm)	GW1N-1	GW1N-2	GW1N-4	GW1N-9	GW1N-1S
CS81M	0.4	4.1 x 4.1				55(15)	
CS30	0.4	2.4 x 2.3	24				23
CM64	0.5	4.1 x 4.1				55(16)	
FN32	0.4	4 x 4					25
CS72	0.4	3.6 x 3.3			57(19)		
QN32	0.5	5 x 5	26		24(3)		
QN48	0.4	6 x 6	41		40(9)	40(12)	
QN48F	0.4	6 x 6				39(11)	
QN88	0.4	10 x 10			70(11)	70(19)	
LQ100	0.5	14 x 14	79	80(15)	79(13)	79(20)	
LQ100X	0.5	14 x 14	79				
LQ144	0.5	20 x 20	116	114(27)	119(22)	120(28)	
LQ144X	0.5	20 x 20					
EQ144	0.5	20 x 20				120(28)	
EQ176	0.4	20 x 20				147(37)	
LQ176	0.4	20 x 20				147(37)	
MG100	0.5	5 x 5				87(25)	
MG121X	0.5	6 x 6		100(28)			
MG132X	0.5	8 x 8		105(28)	105(23)		
MG160	0.5	8 x 8			131(25)	131(38)	
MG196	0.5	8 x 8				113(35)	
PG256	1.0	17 x 17			207(32)	207(36)	
PG256M	1.0	17 x 17			207(32)		
UG169	0.8	11 x 11				129(38)	
UG256	0.8	14 x 14				207(36)	
UG332	0.8	17 x 17				273(43)	

LittleBee GW1NR with On-Chip Memory

On-Chip Memory up to 128Mbits* (16KBytes) *package dependent

Resource	GW1NR-1	GW1NR-4/4B	GW1NR-9
LUT4	1152	4608	8640
Flip-Flop	864	3456	6480
Shadow S-SRAM (Bits)	-	-	17280
Block B-SRAM (Bits)	72K	180K	468K
B-SRAM Blocks	4	10	26
User Flash (Bits)	96K	256K	608K
Memory SDR SDRAM (Bits)	-	64M (QN88)	64M (QN88)
Memory DDR pSRAM (Bits)	-	32M (QN88P) 64M (MG81P)	64M (QN88P/LQ144P/MG100PT/MG100PS) 128M (MG100P/MG100PF/MG100PA)
Memory NOR Flash (Bits)	4M (FN32G)	-	-
Mult 18x18	-	16	20
PLLs	1	2	2
Max I/O	120	218	276
Core Voltage LV	1.2V	1.2V	1.2V
Core Voltage UV	-	2.5V/3.3V	2.5V/3.3V



On-Chip Memory

System-in-Package (SiP) Technology

Package	Pitch (mm)	Size (mm)	GW1NR-1	GW1NR-4	GW1NR-9
QN88	0.4	10 x 10	-	70(11)	70(19)
QN88P	0.4	10 x 10	-	70(11)	70(17)
MG81P	0.5	4.5 x 4.5	-	68(10)	-
MG100P	0.5	5 x 5	-	-	87(16)
MG100PF	0.5	5 x 5	-	-	87(16)
MG100PA	0.5	5 x 5	-	-	87(17)
MG100PT	0.5	5 x 5	-	-	87(17)
MG100PS	0.5	5 x 5	-	-	87(17)
LQ144P	0.5	20 x 20	-	-	120(20)
FN32G	0.4	4 x 4	26	-	-

LittleBee µSoC GW1NS Family

ARM Cortex-M3*, USB-PHY*, ADC*, On-Chip Memory* *package dependent

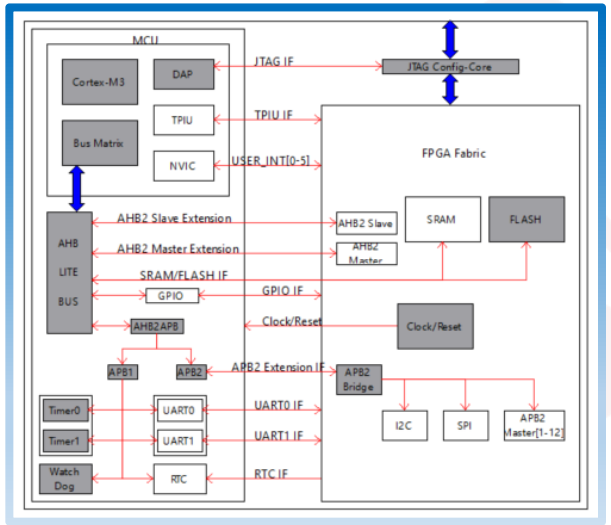
Resource	GW1NS-2 GW1NS-2C*	GW1NSR-2 GW1NSR-2C*	GW1NS-4 GW1NS-4C*	GW1NSR-4 GW1NSR-4C*
LUT4	1728	1728	4608	4608
Flip-Flop	1296	1296	3456	3456
Block B-SRAM (bits)	72K	72K	180K	180K
B-SRAM Blocks	4	4	10	10
User Flash (Bits)	1M	1M	256K	256K
Memory DDR HyperRAM (Bits)	-	-	-	64M (QN48P) *4C Version Only
Memory DDR pSRAM (Bits)	-	32M (QN48P)	-	64M (MG64P)
Memory NOR Flash (Bits)	-	-	-	32M (QN48G) *4C Option Only
Mult 18x18	-	-	16	16
PLLs	1	1	2	2
ARM Cortex-M3	*2C Option	*2C Option	*4C Option	*4C Option
USB PHY	1	1	-	-
ADC	1	1	-	-
Max I/O	102	102	106	106
Core Voltage LV	1.2V	1.2V	1.2V	1.2V

Hardcore
ARM Cortex-M3

MIPI DPHY
I3C

USB-PHY

ADC
8CH, 12-Bit SAR,
1MSamples/s



Package	Pitch(mm)	Size(mm)	GW1NS-2/ GW1NS-2C	GW1NS-4	GW1NS-4C	GW1NSR-2/ GW1NSR-2C	GW1NSR-4	GW1NSR-4C
CS36	0.4	2.5 x 2.5	30(6)					
CS49	0.4	2.9 x 2.9		42(8)	42(8)			
QN32	0.5	5 x 5	25(4)					
QN32U	0.5	5 x 5	16(2)					
QN48	0.4	6 x 6	38(7)	38(4)	38(4)			
LQ144	0.5	20 x 20	95(12)					
QN48P	0.4	6 x 6				38(7)		39(4)
QN48G	0.4	6 x 6						39(4)
MG64	0.5	4.2 x 4.2			57(8)			
MG64P	0.5	4.2 x 4.2					55(8)	55(8)

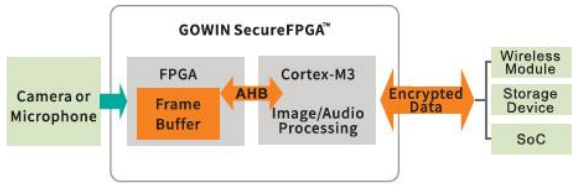
LittleBee µSoC GW1NSE SecureFPGA

SecureFPGA Root-of-Trust using Physically Unclonable Functionality (PUF) Technology

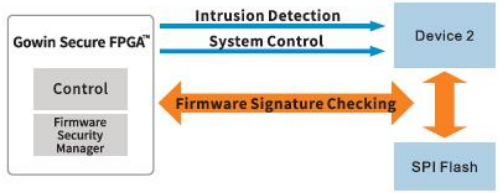
Applications of LittleBee® GW1NSE

Typical Applications:

IoT camera module or microphone array application:



Firmware encryption application:



Device	GW1NSE-2C	GW1NSE-4C	GW1NSER-4C
LUT4	1728	4608	4,608
Flip-Flop	1296	3456	3,456
B-SRAM (bits)	72K	180K	180K
Number of B-SRAM	4	10	10
S-SRAM (bits)	4608	0	-
User Flash (bits)	1024	256	256K
HyperRAM(bits)	-	-	64M
NOR FLASH(Mbits)	-	-	32M
18 x 18 Multiplier	-	16	16
PLLs	1	2	2
OSC	1, ±5% accuracy	1, ±5% accuracy	1, ±5% accuracy
Hard Core Processor	Cortex-M3	Cortex-M3	Cortex-M3
USB 2.0 PHY	1	0	-
ADC Channels	8	0	
I/O Banks	4	3	4
Max. I/O on die	102	106	106
Core Voltage	1.2V	1.2V	1.2V

Package	Pitch(mm)	Size(mm)	GW1NSE-2C	GW1NSER-2C	GW1NSER-4C
QN48	0.4	6 x 6	39(7)		
LQ144	0.5	20 x 20	91(11)		
QN48P	0.4	6 x 6			38(4)
QN48G	0.4	6 x 6			38(4)

LittleBee GW1NZ Ultra-Low Power

Ultra-Low Power, Lowest Cost, Flash-Based, Non-Volatile, Instant On

Zero Power

Extremely Small Package
CS16 1.8mm x 1.8mm

Resource	GW1NZ-1
LUT4	1152
Flip-Flop	864
Block B-SRAM (bits)	72K
B-SRAM Blocks	4
User Flash (Bits)	64K
PLLs	1
Max I/O	48
Core Voltage ZV	0.9V
Core Voltage LV	1.2V

Core Voltage

- **LV** 1.2V **ZV** 0.9V

Power

- Standby < 10uW
- Always On < 28uW

Packagev	Pitch (mm)	Size (mm)	GW1NZ-1
FN32	0.4	4 x 4	25
FN32F	0.4	4 x 4	25
CS16	0.4	1.8 x 1.8	11
QN48	0.4	6 x 6	40

LittleBee GW1NRF Bluetooth Low Energy (BLE)

BLE 5.0, 4K LUTs FPGA, Optimized 32-bit Processor

BLE 5.0
- 4K LUT FPGA
- 32-bit Processor
- **Certified BLE Module**

Power Management
- 5nA Standby
- < 1uA Sleep
- < 5mA Active

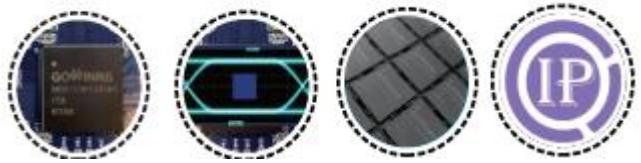
µSoC
- Step Up/Down Regulator
- Embedded FLASH
- Embedded OTP & RAM

Hardened Security
- TRNG
- AES-128
- ECC-P256 Key Gen

FPGA Feature	GW1NRF-4B	SoC Feature	GW1NRF
LUT4	4,606	Bluetooth 5.0 LE	Up to 8 Simultaneous Connections
Flip-Flop	3,456	32-bit ARC Processor	24MHz
Shadow SRAM S-RAM (bits)	-	Processor ROM (Bytes)	136K
Block SRAM B-SRAM (bits)	180K	Processor OTP (Bytes)	128K
Number of B-SRAM Blocks	10	Processor IRAM/DRAM (Bytes)	48K / 28K
User Flash (bits)	256K	Security Core	TRNG, AES-128, ECC-P256
Multipliers 18 x 18	16	Power Management	Scheduler & Memory Manager
PLLs + DLLs	2 + 2	DC-to-DC Step-Up/ Step-Down Regulator	Supports 1.5V & 3.0V Batteries
I/O Banks	4	**Package**	**Pitch (mm)**
Max User I/O	25	QFN48	0.4
FPGA Core Voltage (LV)	1.2V	**Size (mm^2)**	**User I/O / True LVDS Pairs**
FPGA Core Voltage (UV)	1.8V/2.5V/3.3V	6 x 6	25(4)

Arora GW2A family

55nm SRAM Technology, High Performance DSP, High-Speed LVDS, Abundant B-SRAM



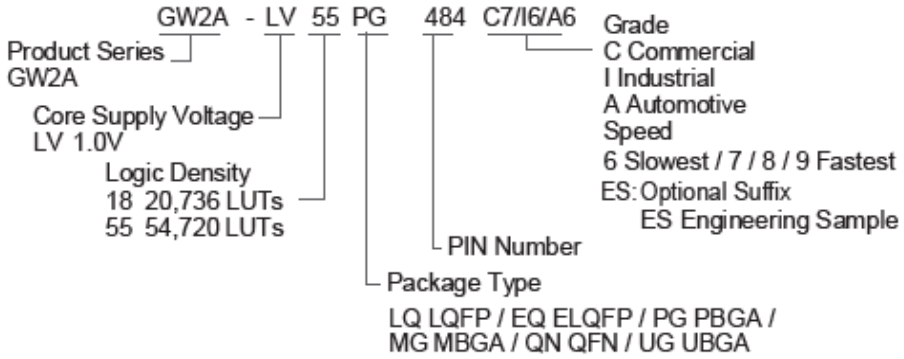
55nm SRAM
Core Voltage: 1.0V

DDR3
RISC-V
CORTEX-M
CAN2.0
Ethernet

Resource	GW2A-18	GW2A-55
LUT4	20.736	54,720
Flip-Flop	15,552	41,040
Shadow S-SRAM (Bits)	41,472	109,440
Block B-SRAM (bits)	828K	2520K
B-SRAM Blocks	46	140
Mult 18x18	48	40
PLLs	4	6
I/O Banks	8	8
Max I/O	384	608
Core Voltage LV	1.0V	1.0V

Package	Pitch(mm)	Size(mm)	E-pad Size(mm)	GW2A-18	GW2A-55
QN88	0.4	10 x 10		66(22)	
LQ144	0.5	20 x 20		119(34)	
EQ144	0.5	20 x 20	9.74 x 9.74	119(34)	
MG196	0.5	8 x 8		114(39)	
UG324	0.8	15 x 15		239(90)	240(86)
UG324D	0.8	15 x 15			240(71)
PG256	1.0	17 x 17		207(73)	
PG256S	1.0	17 x 17		192(72)	
PG256C	1.0	17 x 17		190(64)	
PG256E	1.0	17 x 17		162(29)	
PG484	1.0	23 x 23		319(77)	319(75)
PG1156	1.0	35 x 35			607(96)

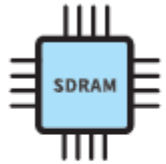
GW2A Part Numbering



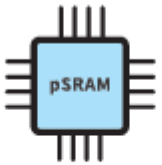
Arora GW2AR Family with On-Chip Memory

16MB DDR SDRAM or 8MB DDR pSRAM or 8MB SDR SDRAM plus 4MB Non-Volatile NOR FLASH

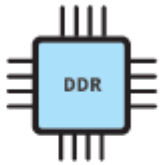
Resource	GW2AR-18	GW2ANR-18
LUT4	20.736	20.736
Flip-Flop	15,552	15,552
Shadow S-SRAM (Bits)	41,472	41,472
Block B-SRAM (bits)	828K	828K
B-SRAM Blocks	46	46
Memory NOR Flash (Bits)	-	32M (QN88)
Memory SDR SDRAM (Bits)	64M (QN88, LQ144, EQ144)	64M (QN88)
Memory DDR SDRAM (Bits)	128M (LQ176, EQ176)	-
Memory DDR pSRAM (Bits)	64M (QN88P, QN88PF, EQ144P, EQ144PF)	-
Mult 18x18	48	48
PLLs	4	4
I/O Banks	8	8
Max I/O	384	384
Core Voltage LV	1.0V	1.0V



64Mbits SDRAM
Bit Width :32bits
Clock Frequency :143MHz



64Mbits pSRAM
Bit Width :16bits
Clock Frequency :166MHz
Double edge data



128Mbits DDR
Bit Width :16bits
Clock Frequency : 200MHz
Double edge data transmission

Package	Pitch(mm)	Size(mm)	E-pad Size(mm)	GW2AR-18	GW2ANR-18
LQ144	0.5	20 x 20		120(35)	
EQ144	0.5	20 x 20	9.74 x 9.74	120(35)	
EQ144P	0.5	20 x 20	9.74 x 9.74	120(35)	
EQ144PF	0.5	20 x 20	9.74 x 9.74	120(35)	
QN88	0.4	10 x 10	6.74 x 6.74	66(22)	66(22)
QN88P	0.4	10 x 10	6.74 x 6.74	66(22)	
QN88PF	0.4	10 x 10	6.74 x 6.74	66(22)	
LQ176	0.4	20 x 20		140(45)	
EQ176	0.4	20 x 20	6 x 6	140(45)	

Note: LQ144 and QN88 integrate 64M SDR SDRAM; LQ176 integrates 128M DDR SDRAM

Arora GW2AN-18 with On-Chip Flash – Available Q1 2021

Adds I²C Configuration, 2MB Non-Volatile NOR FLASH, Supports Background Updates & Programming

Resource	GW2AN-18
LUT4	20.736
Flip-Flop	15,552
Shadow S-SRAM (Bits)	41,472
Block B-SRAM (bits)	540K
B-SRAM Blocks	30
Memory NOR Flash (Bits) 2-bit streams	16Mb
Mult 18x18	48
PLLs	4
LVDS Bandwidth (per lane)	1.25Gbps
MIPI Bandwidth (per lane)	1.2Gbps
I/O Banks	8
Max I/O	384
Core Voltage EV	1.0V
Core Voltage LV	1.2V
Core Voltage UV	2.5V / 3.3V

Adds I²C Programming Support

Supports 5 Configuration Modes

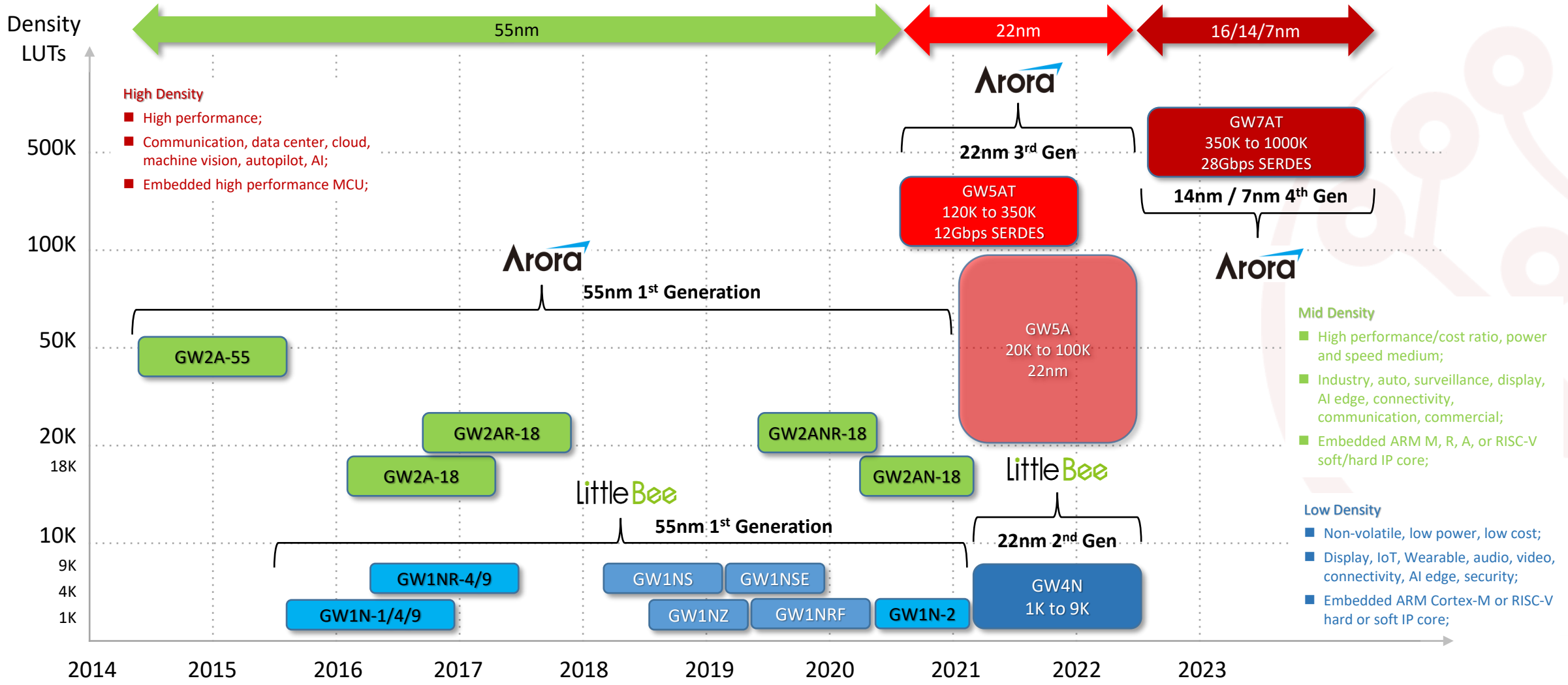
- JTAG, CPU, I²C, SSPI, SERIAL, Autoboot

Dual Partition NOR Flash

- Supports Autoboot (Non-volatile)
- Supports Background Updates & Programming
- Update & Switch Images while device is active

Package	Pitch (mm)	Size (mm)	GW2AN-18
PG256	1.0	17 x 17	206
UG256	0.8	14 x 14	206
UG324	0.8	15 x 15	279
UG332	0.8	17 x 17	278
UG400	0.8	17 x 17	335
UG484	0.8	19 x 19	384

GOWIN Product Roadmap



GOWIN FPGA Embedded Processors

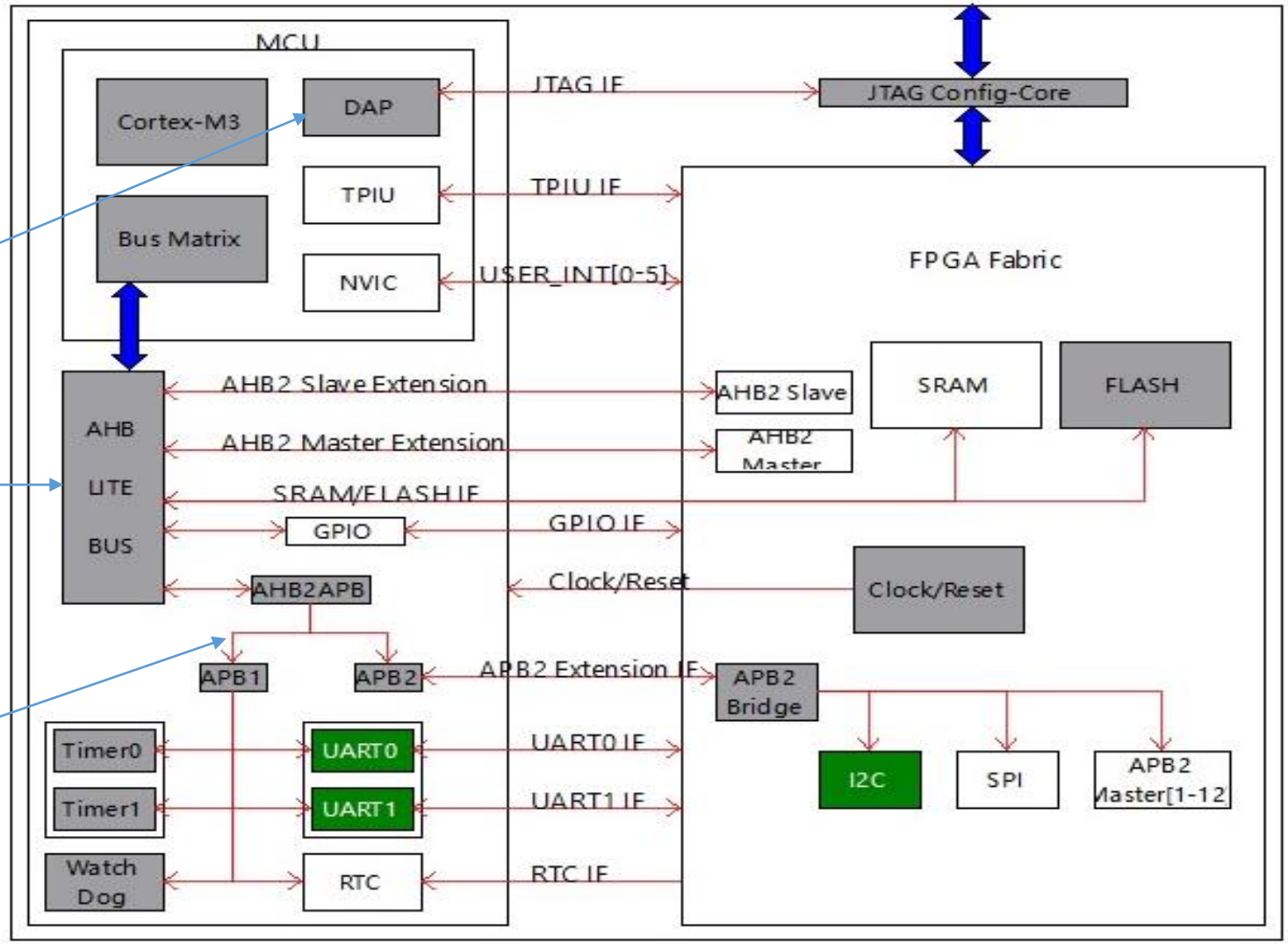
GOWIN FPGA Embedded Processor Options					
Core	**Instruction Set**	**IP Resources (LUTs)**	**DMIPS/MHz**	**CoreMark®/MHz**	**Device Family / CLK Freq (MHz)**
PicoRV32	RISC-V	Softcore 2K	0.516	-	GW2A*: 50 GW1N* : 50
Andes N25	RISC-V AndeStar™ V5	Softcore 10K	GW2A18: 1.94 GW2A55: 2.29	-	GW2A*: 50
Cortex M1	ARM Thumb, Thumb-2	Softcore (5K to 21K)	0.8	1.85	GW2A*: 75 GW1N9: 40
Cortex M3	ARM Thumb, Thumb-2	Softcore (18K to 37K)	1.25 to 1.89	3.34	GW2A55: 25
Cortex M3	ARM Thumb, Thumb-2	Hardcore N/A	1.25 to 1.89	3.34	GW1NS*-2C: 30 GW1NS*-4C: 100
ARC EM4	Synopsys ARCv2	Hardcore N/A	1.77	3.41	GW1NRF: 24

Hard M3 core

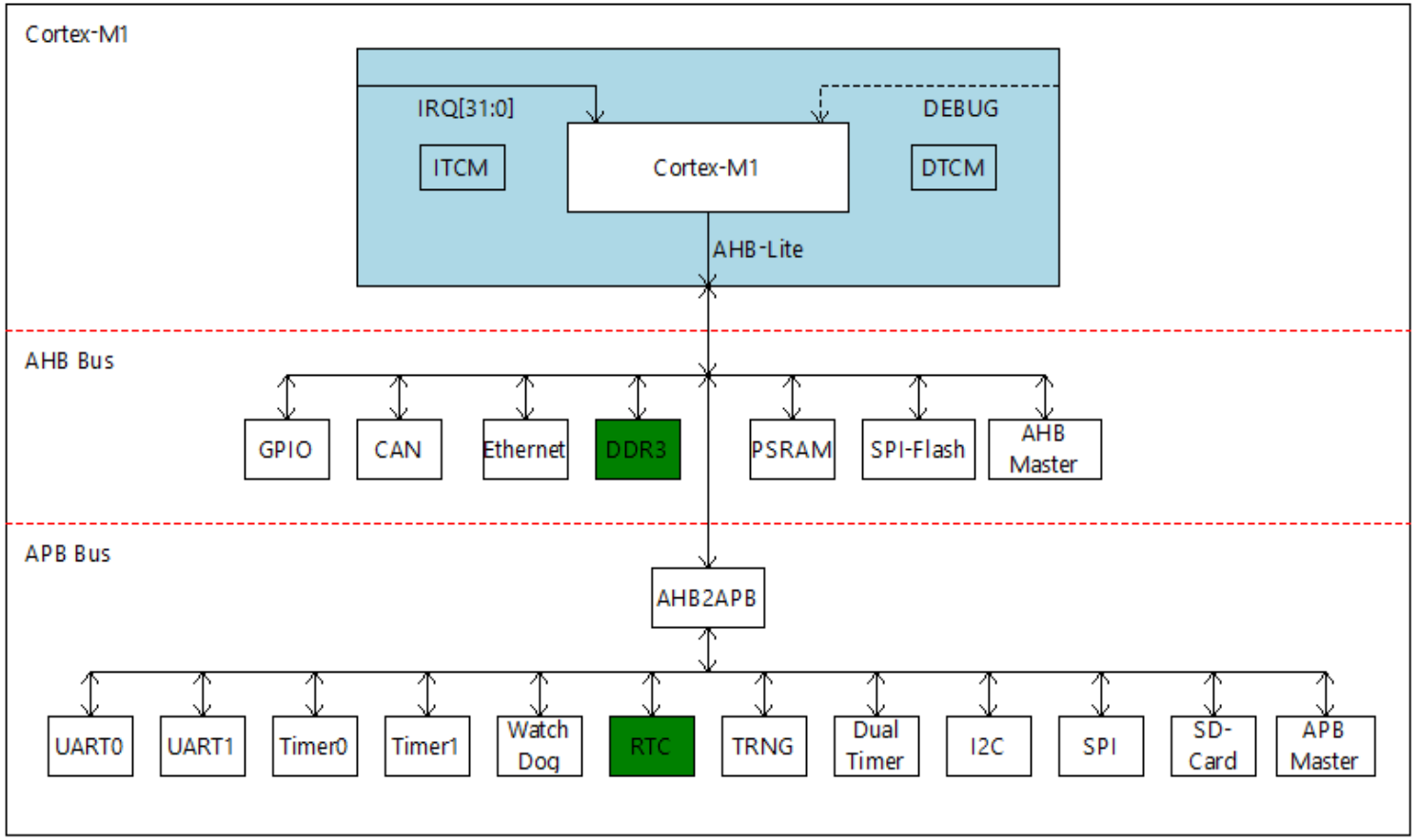
Debug port

High speed bus

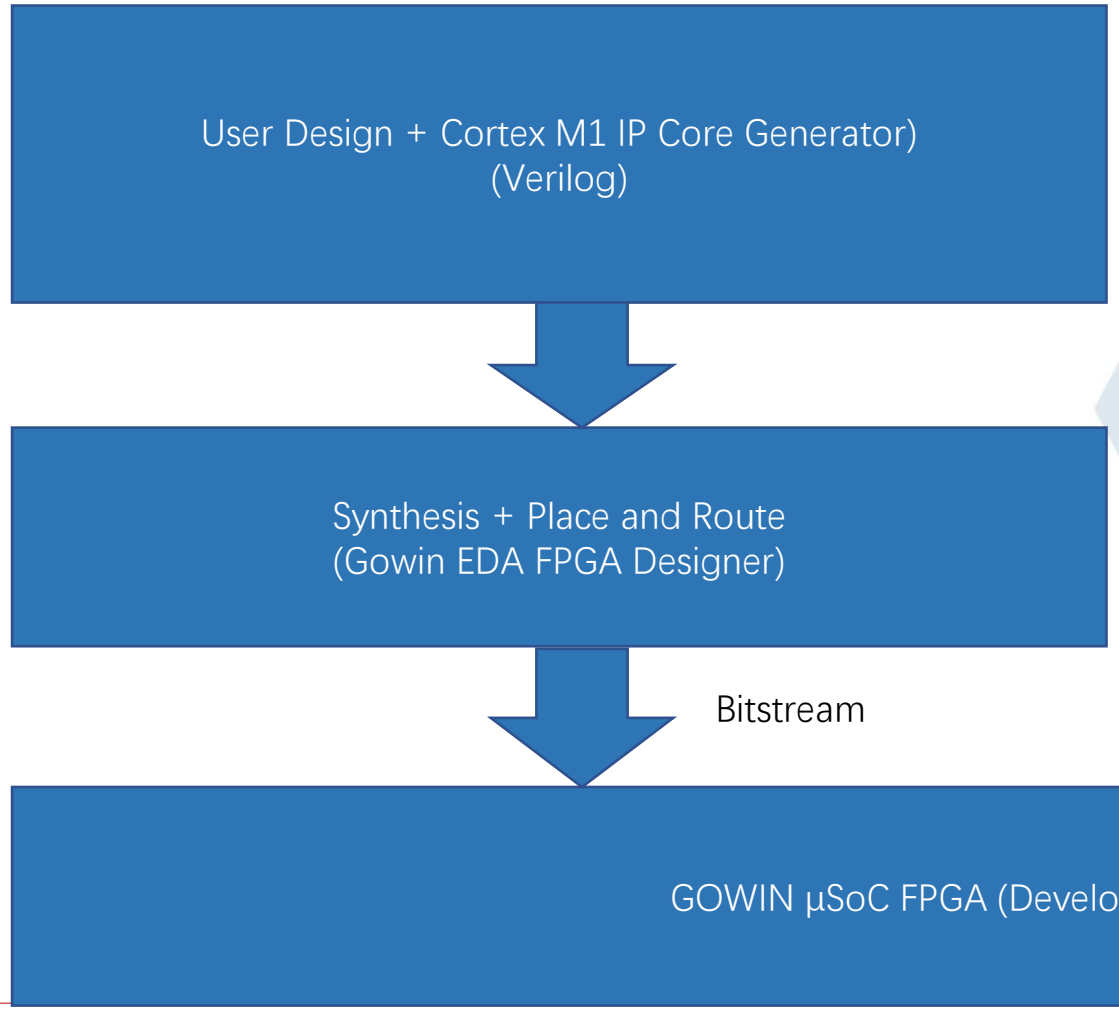
Peripheral (low speed) bus



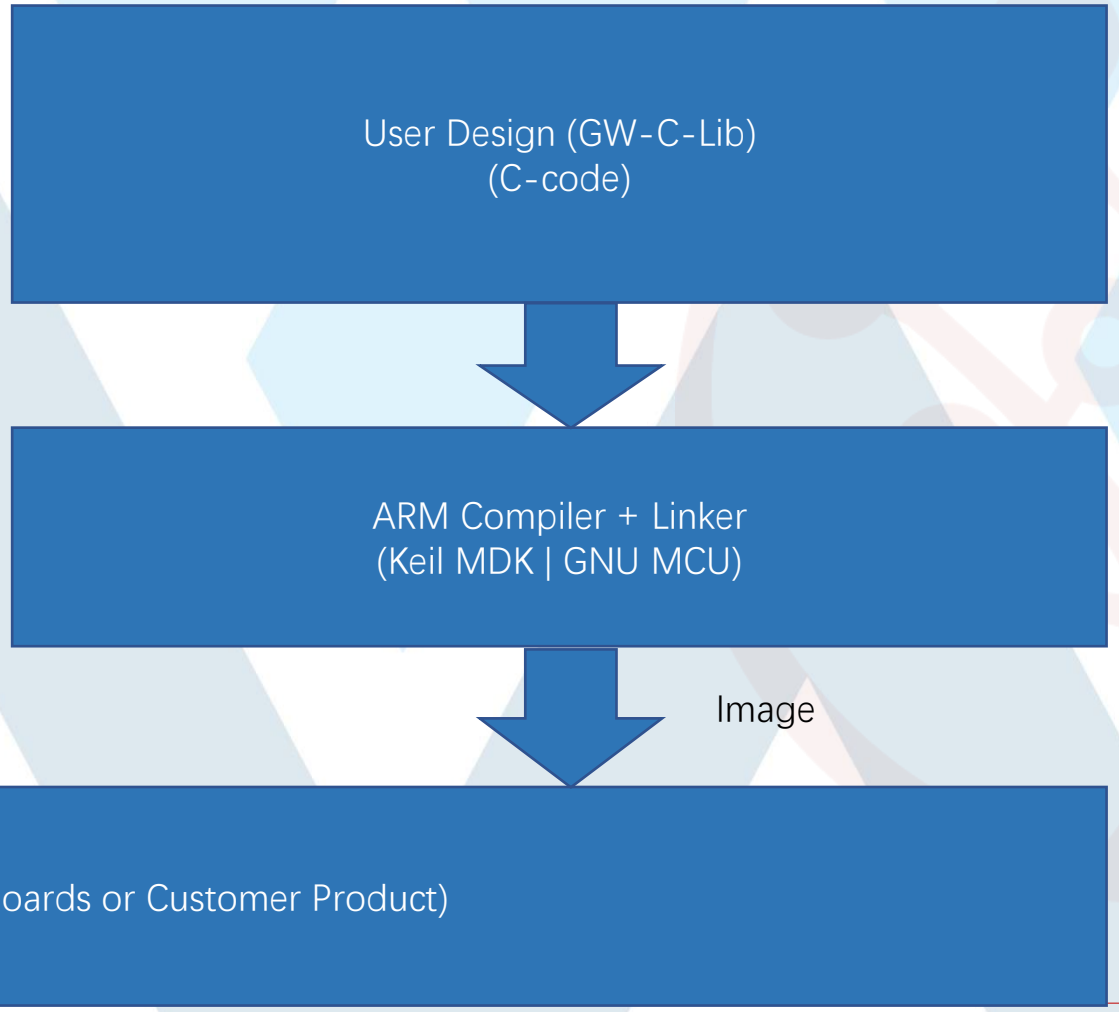
Soft M1 core


Cortex-M1
IRQ[31:0]
DEBUG
ITCM
Cortex-M1
DTCM
AHB-Lite
AHB Bus
GPIO
CAN
Ethernet
DDR3
PSRAM
SPI-Flash
AHB Master
APB Bus
AHB2APB
UART0
UART1
Timer0
Timer1
Watch Dog
RTC
TRNG
Dual Timer
I2C
SPI
SD-Card
APB Master

FPGA Design Flow

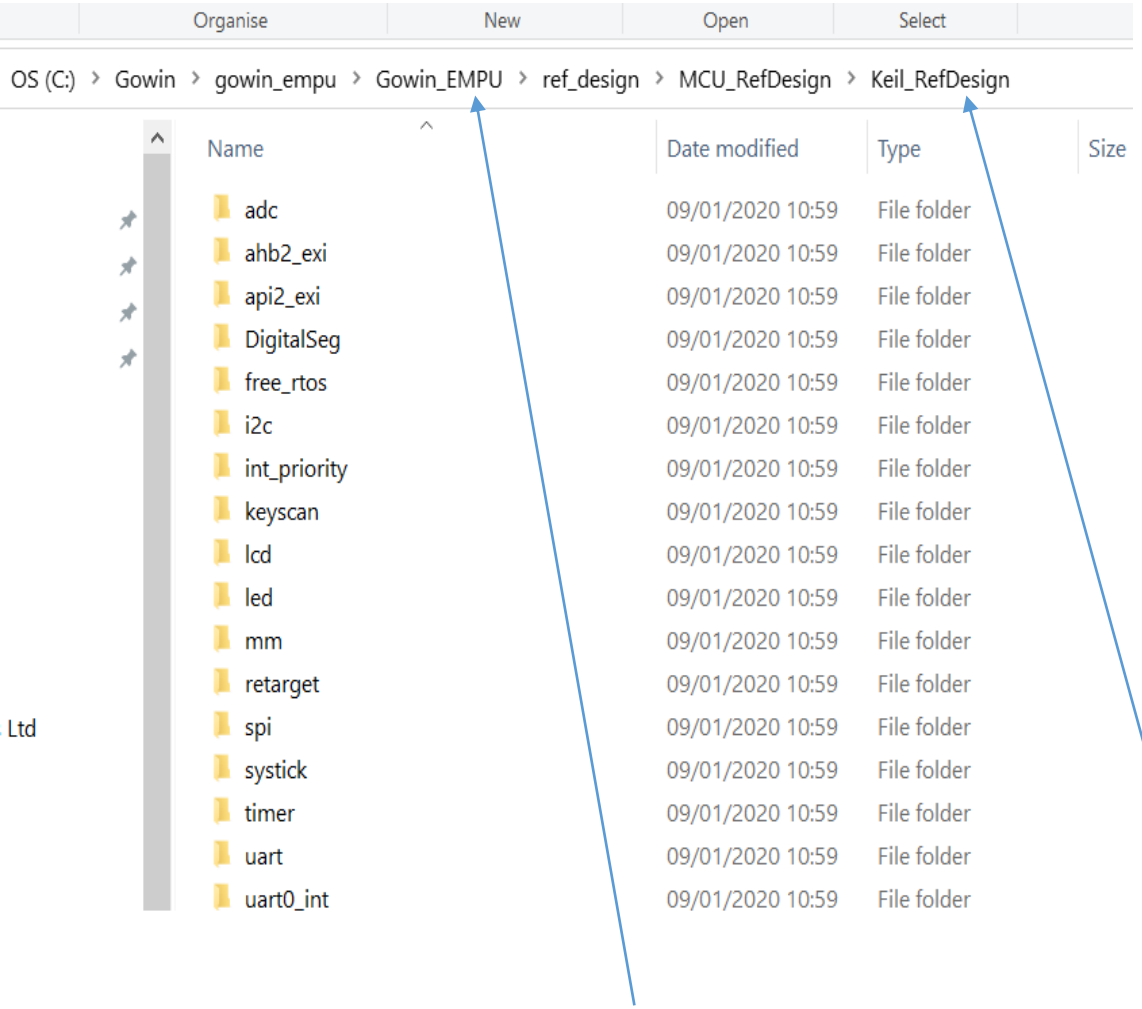


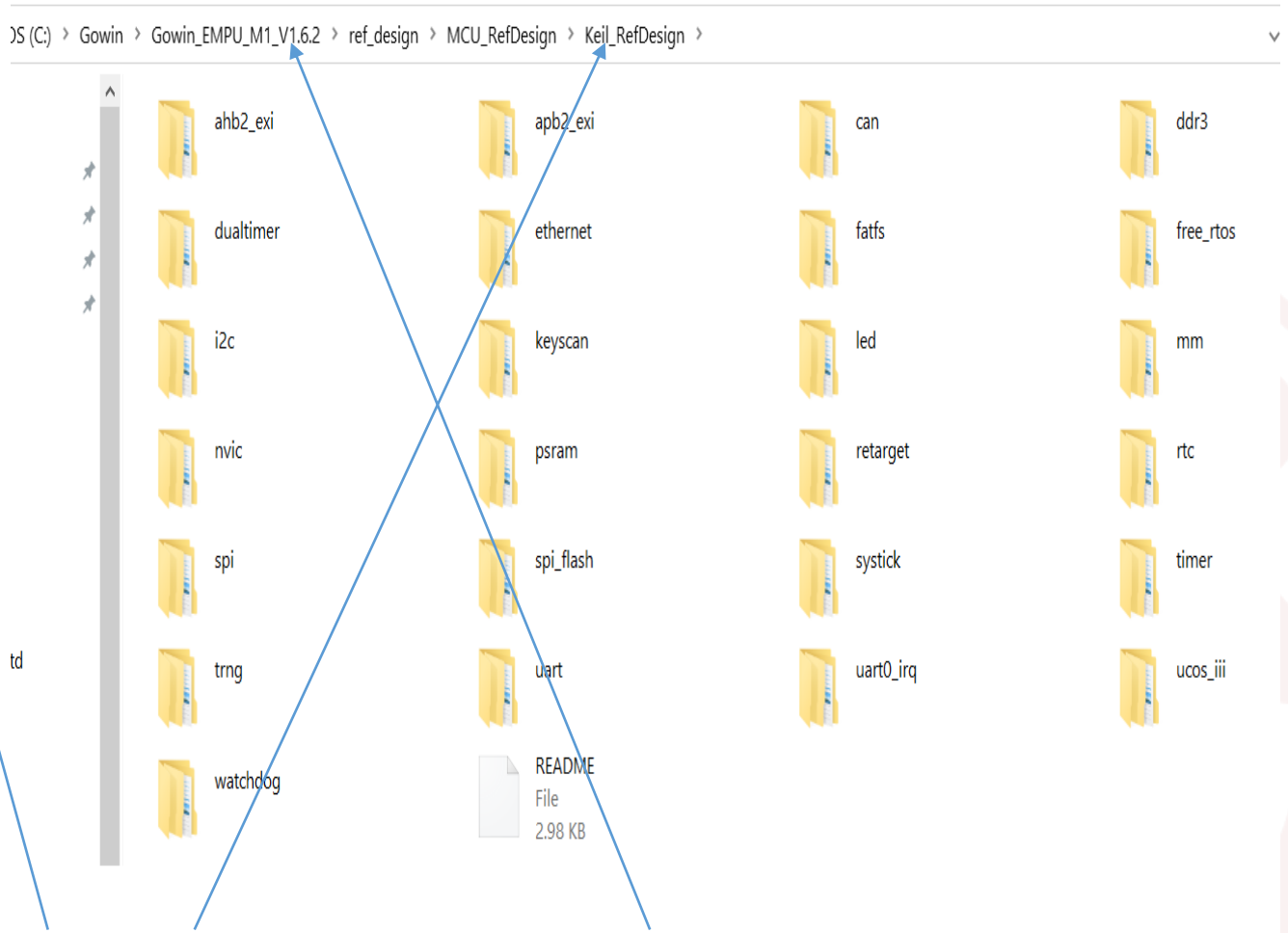
Software Design Flow



GOWIN µSoC FPGA (Development Boards or Customer Product)

EMPU software ref designs



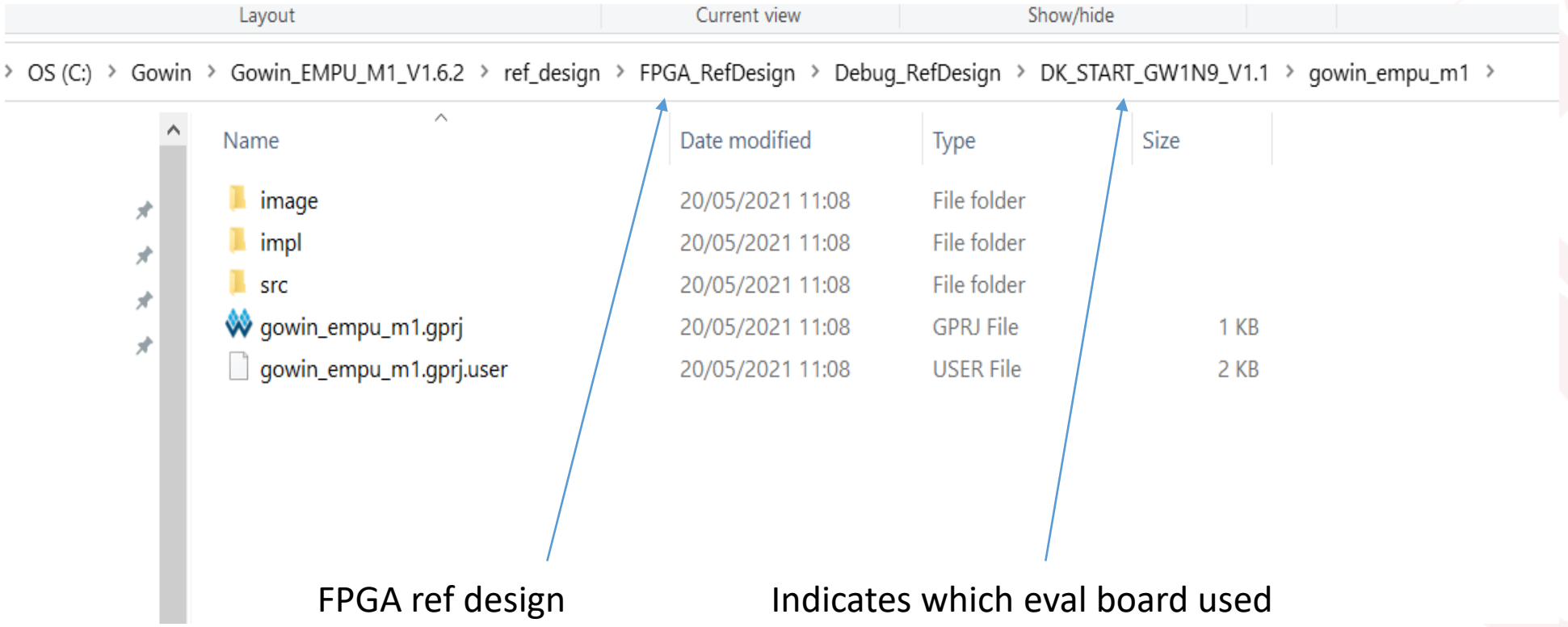


Hard core

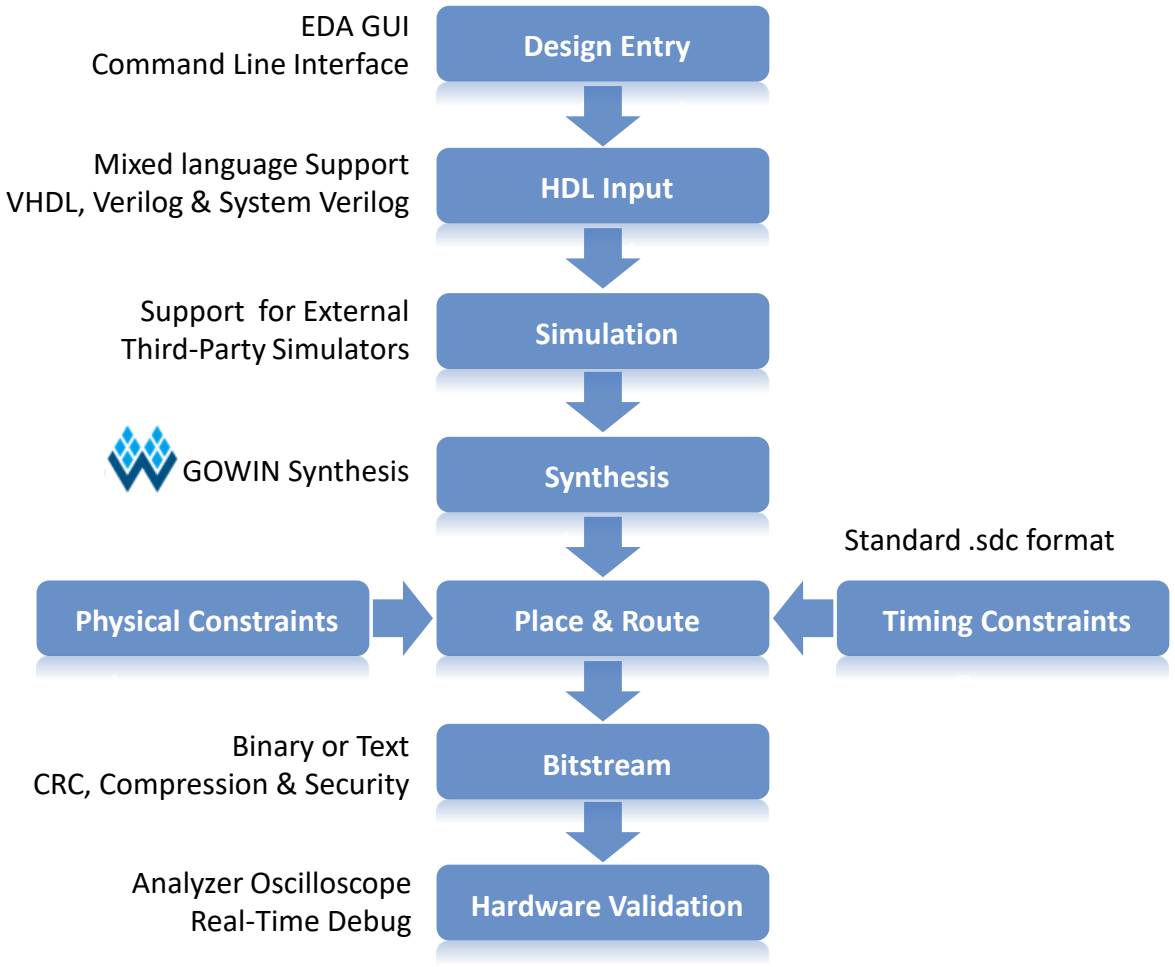
S\W ref design

Soft core

EMPU FPGA ref designs



GOWIN EDA® FPGA Designer



Operating System

- Windows or Linux (inc. Ubuntu)

Freely Licensed

- Fixed or Floating Licenses

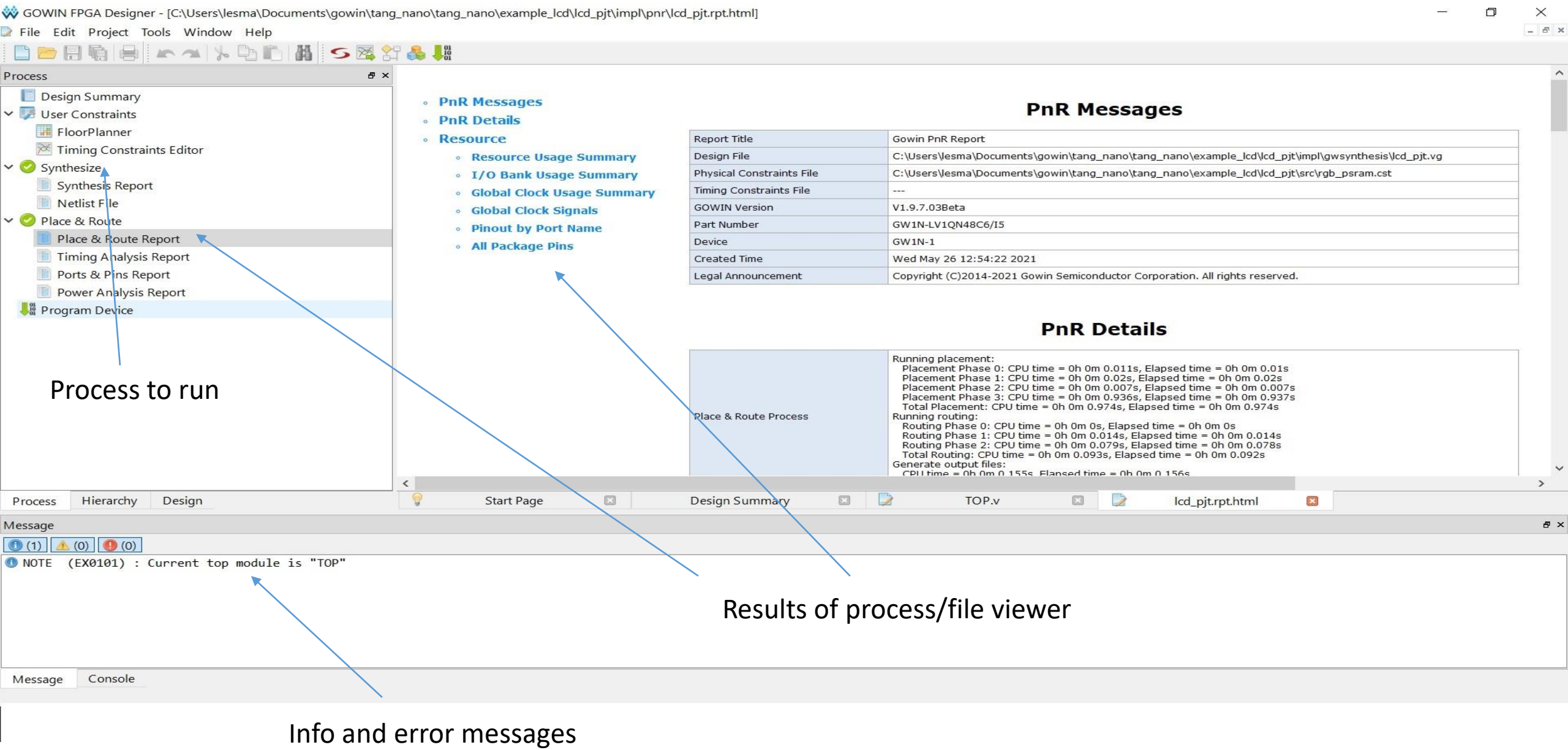
Easy-of-Use

- Very Intuitive & Familiar Looking

Fully Featured Tool Chain

- Free IP Core Generator
- Floor-Planner
- Timing Constraints Editor
- Schematic Viewer
- Hierarchy Viewer
- GOWIN Analyzer Oscilloscope
- Project Archiving
- Module Encryption
- Standalone Programmer

GoWin EDA tool – Process view

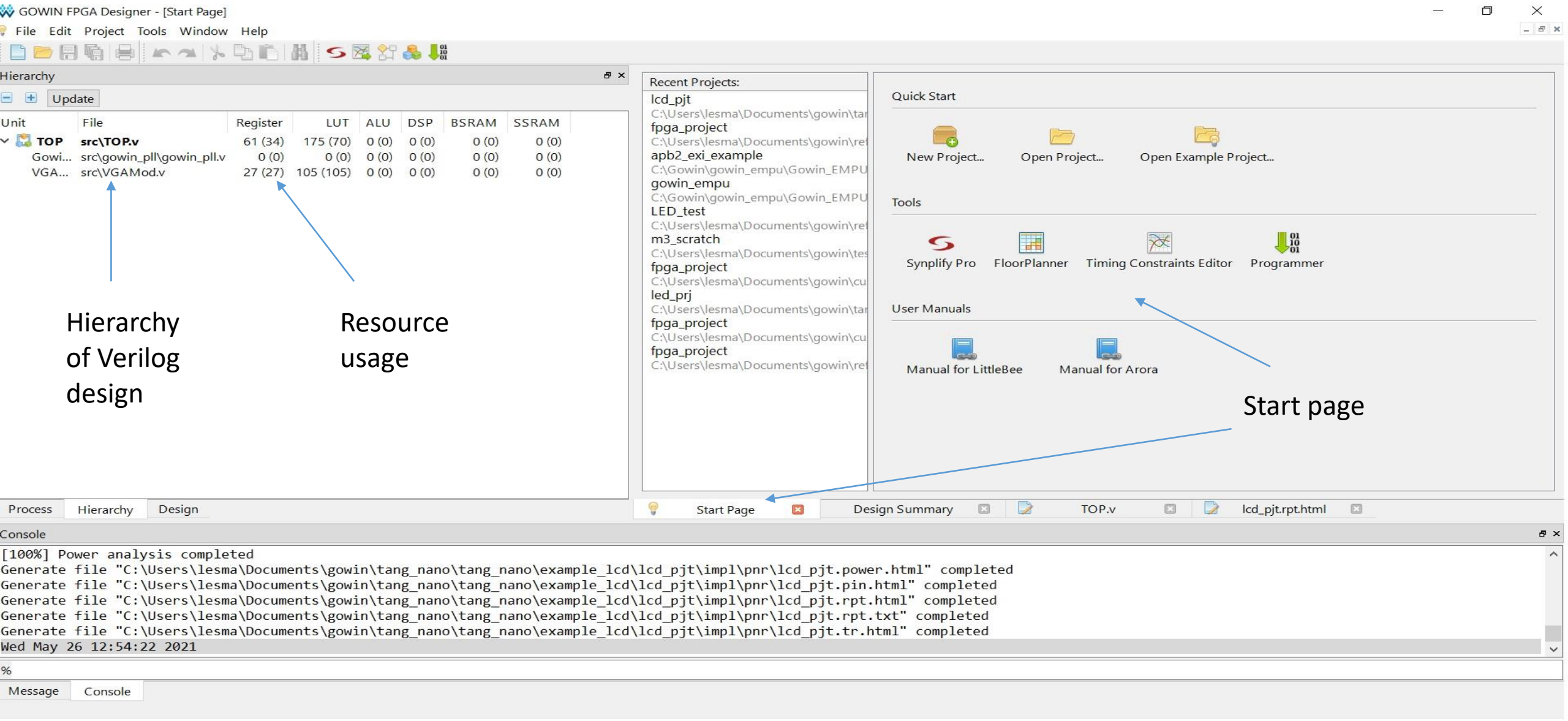


Process to run

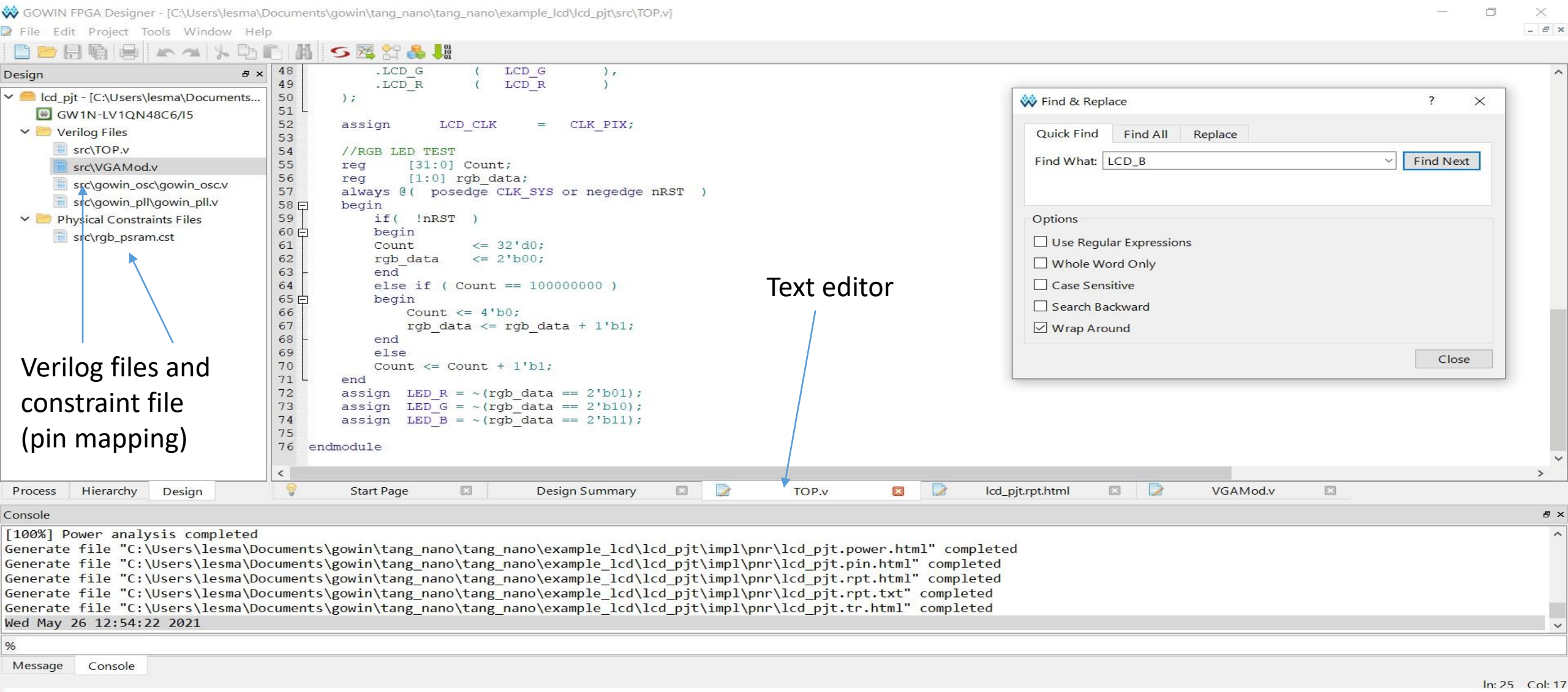
Results of process/file viewer

Info and error messages

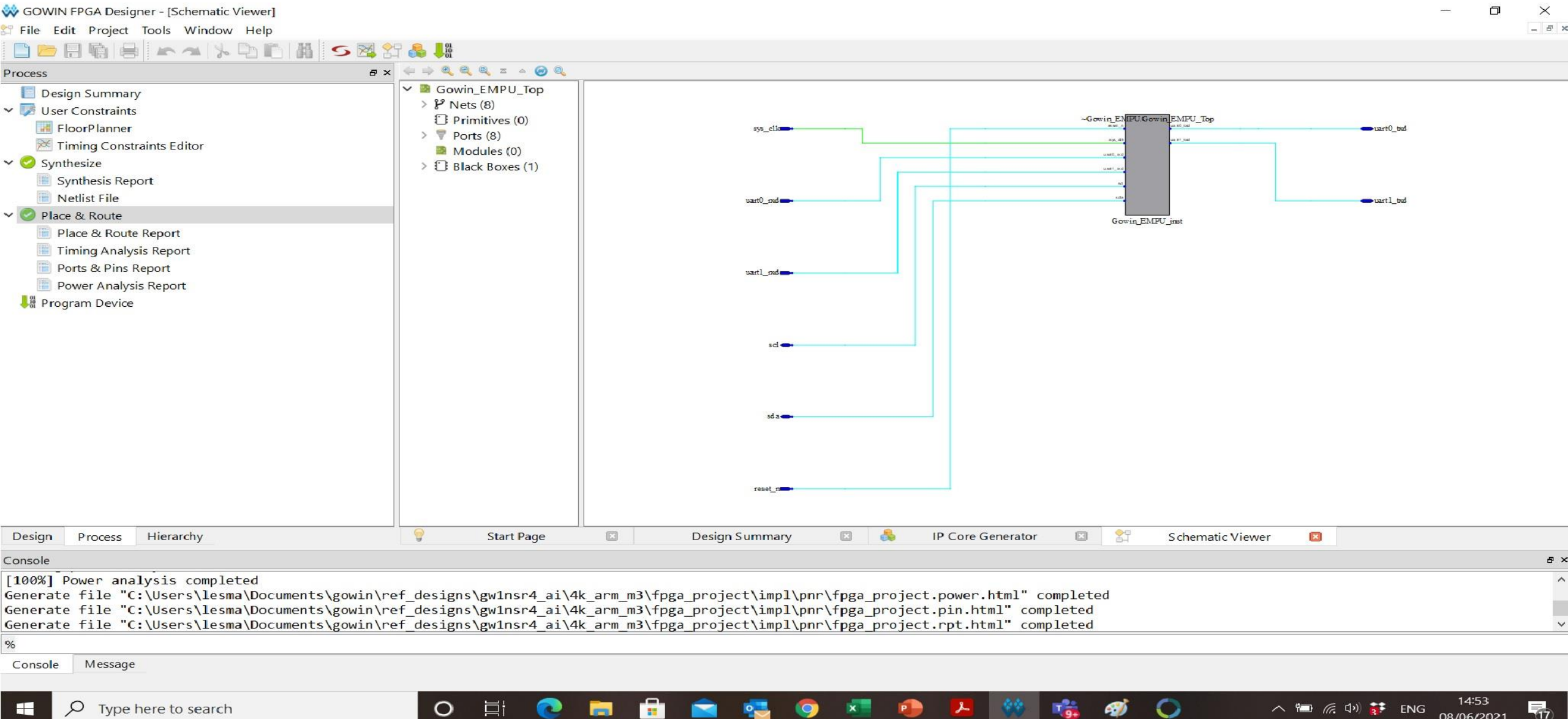
Hierarchy View



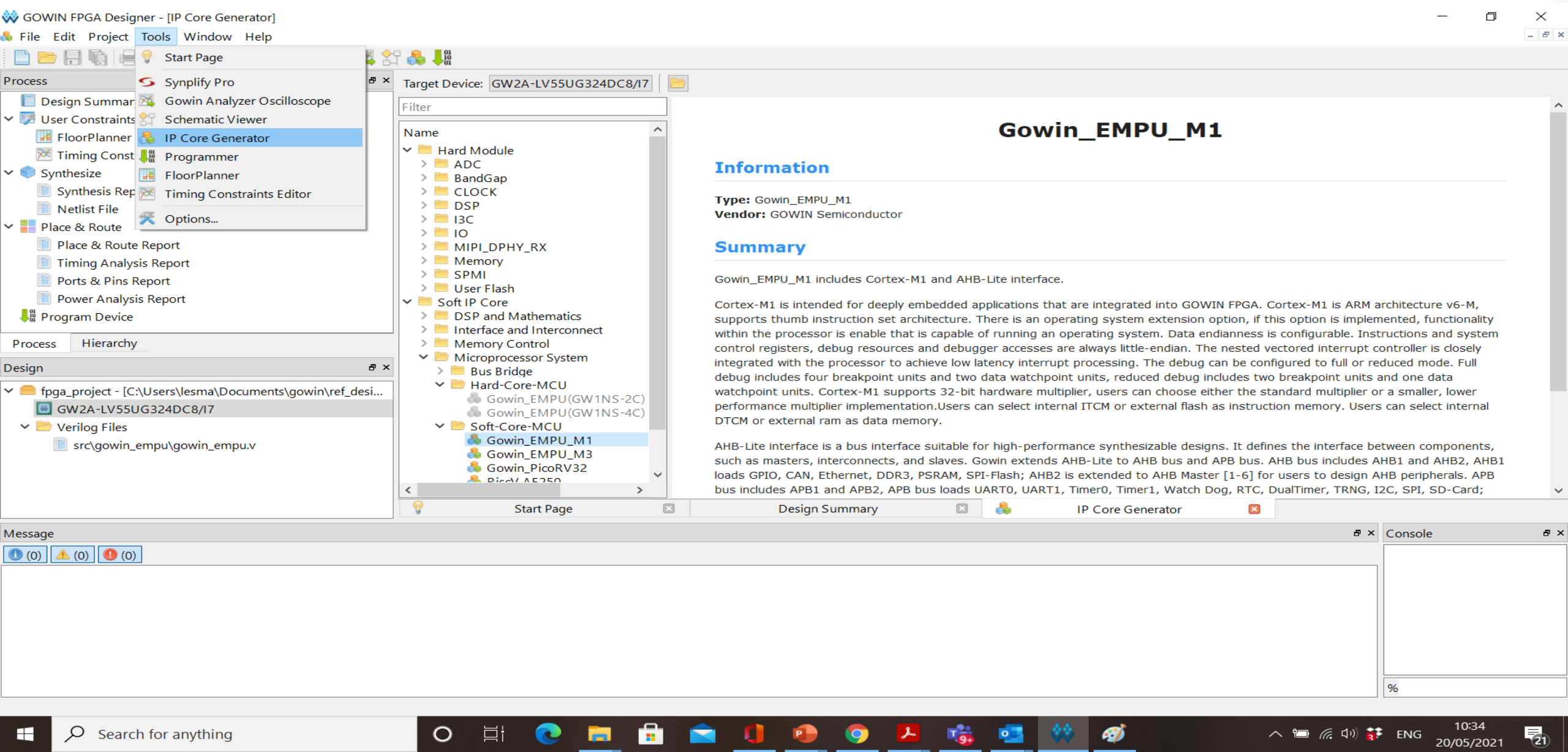
Design view


GOWIN FPGA Designer - [C:\Users\lesma\Documents\gowin\tang_nano\tang_nano\example_lcd\lcd_pjt\src\TOP.v]
File Edit Project Tools Window Help
Design
lcd_pjt - [C:\Users\lesma\Documents...
GW1N-LV1QN48C6/I5
Verilog Files
src\TOP.v
src\VGAMod.v
src\gowin_osc\gowin_osc.v
src\gowin_pll\gowin_pll.v
Physical Constraints Files
src\rgb_psram.cst
Verilog files and constraint file (pin mapping)
Text editor
Find & Replace
Quick Find
Find All
Replace
Find What: LCD_B
Find Next
Options
Use Regular Expressions
Whole Word Only
Case Sensitive
Search Backward
Wrap Around
Close
Process
Hierarchy
Design
Start Page
Design Summary
TOP.v
lcd_pjt.rpt.html
VGAMod.v
Console
[100%] Power analysis completed
Generate file "C:\Users\lesma\Documents\gowin\tang_nano\tang_nano\example_lcd\lcd_pjt\impl\pnr\lcd_pjt.power.html" completed
Generate file "C:\Users\lesma\Documents\gowin\tang_nano\tang_nano\example_lcd\lcd_pjt\impl\pnr\lcd_pjt.pin.html" completed
Generate file "C:\Users\lesma\Documents\gowin\tang_nano\tang_nano\example_lcd\lcd_pjt\impl\pnr\lcd_pjt.rpt.html" completed
Generate file "C:\Users\lesma\Documents\gowin\tang_nano\tang_nano\example_lcd\lcd_pjt\impl\pnr\lcd_pjt.rpt.txt" completed
Generate file "C:\Users\lesma\Documents\gowin\tang_nano\tang_nano\example_lcd\lcd_pjt\impl\pnr\lcd_pjt.tr.html" completed
Wed May 26 12:54:22 2021
Message
Console
Ln: 25 Col: 17

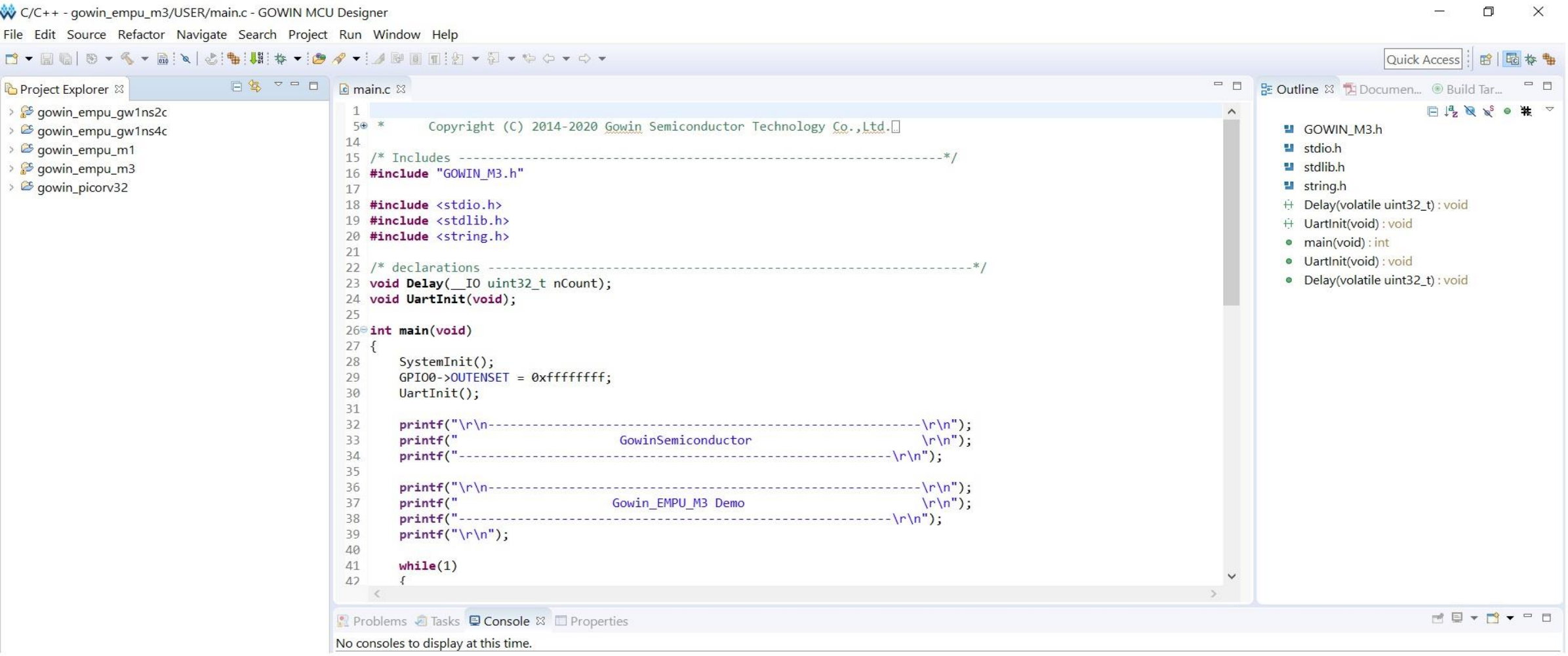
Schematic viewer



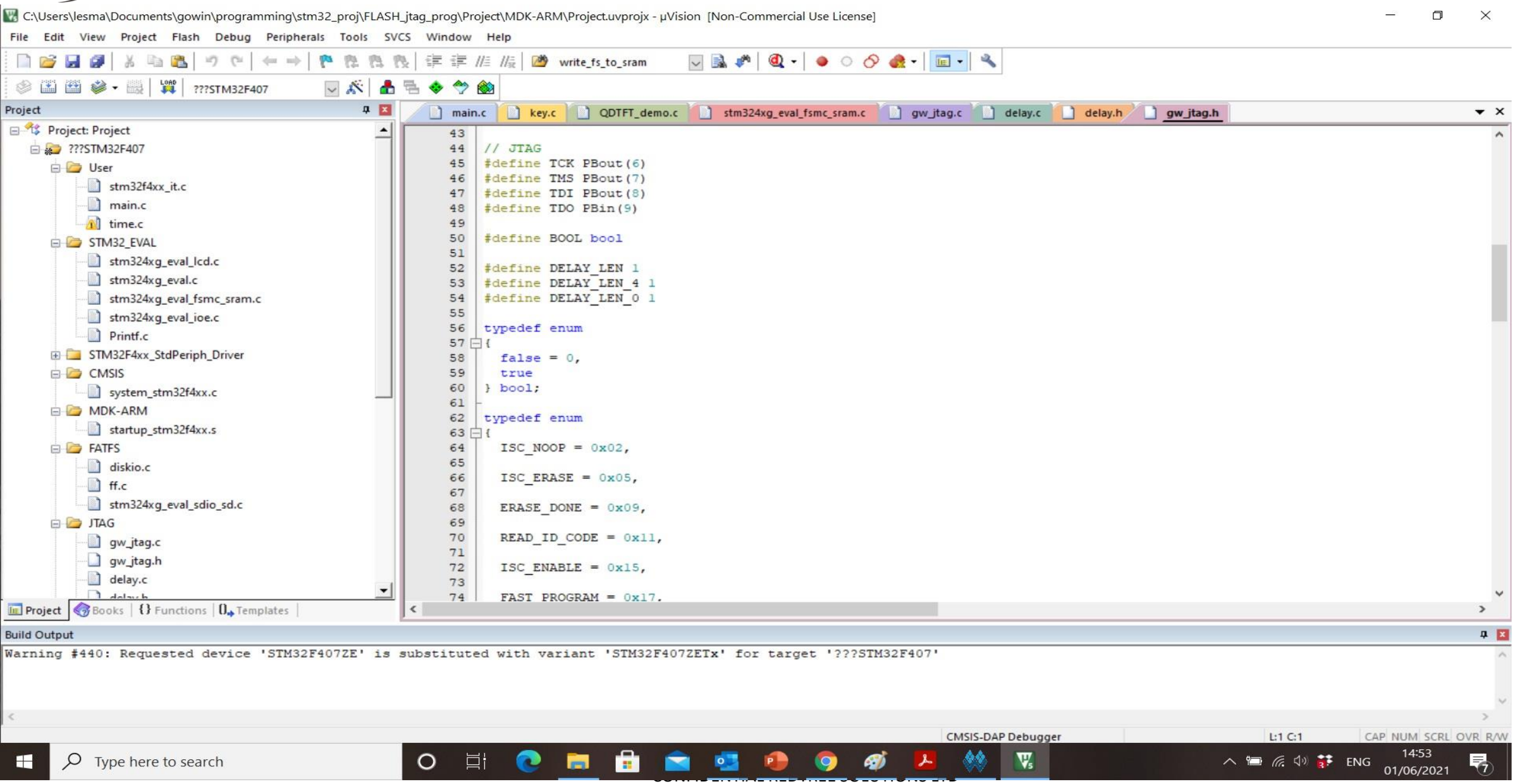
Other tools


GOWIN FPGA Designer - [IP Core Generator]
File Edit Project Tools Window Help
Start Page
Synplify Pro
Gowin Analyzer Oscilloscope
Schematic Viewer
IP Core Generator
Programmer
FloorPlanner
Timing Constraints Editor
Options...
Process
Design Summar
User Constraints
FloorPlanner
Timing Const
Synthesize
Synthesis Rep
Netlist File
Place & Route
Place & Route Report
Timing Analysis Report
Ports & Pins Report
Power Analysis Report
Program Device
Process Hierarchy
Design
fpga_project - [C:\Users\lesma\Documents\gowin\ref_desi...
GW2A-LV55UG324DC8/I7
Verilog Files
src\gowin_empu\gowin_empu.v
Target Device: GW2A-LV55UG324DC8/I7
Filter
Name
Hard Module
ADC
BandGap
CLOCK
DSP
I3C
IO
MIPI_DPHY_RX
Memory
SPMI
User Flash
Soft IP Core
DSP and Mathematics
Interface and Interconnect
Memory Control
Microprocessor System
Bus Bridge
Hard-Core-MCU
Gowin_EMPU(GW1NS-2C)
Gowin_EMPU(GW1NS-4C)
Soft-Core-MCU
Gowin_EMPU_M1
Gowin_EMPU_M3
Gowin_PicoRV32
Gowin_EMPU_M1
Information
Type: Gowin_EMPU_M1
Vendor: GOWIN Semiconductor
Summary
Gowin_EMPU_M1 includes Cortex-M1 and AHB-Lite interface.
Cortex-M1 is intended for deeply embedded applications that are integrated into GOWIN FPGA. Cortex-M1 is ARM architecture v6-M, supports thumb instruction set architecture. There is an operating system extension option, if this option is implemented, functionality within the processor is enable that is capable of running an operating system. Data endianness is configurable. Instructions and system control registers, debug resources and debugger accesses are always little-endian. The nested vectored interrupt controller is closely integrated with the processor to achieve low latency interrupt processing. The debug can be configured to full or reduced mode. Full debug includes four breakpoint units and two data watchpoint units, reduced debug includes two breakpoint units and one data watchpoint units. Cortex-M1 supports 32-bit hardware multiplier, users can choose either the standard multiplier or a smaller, lower performance multiplier implementation.Users can select internal ITCM or external flash as instruction memory. Users can select internal DTCM or external ram as data memory.
AHB-Lite interface is a bus interface suitable for high-performance synthesizable designs. It defines the interface between components, such as masters, interconnects, and slaves. Gowin extends AHB-Lite to AHB bus and APB bus. AHB bus includes AHB1 and AHB2, AHB1 loads GPIO, CAN, Ethernet, DDR3, PSRAM, SPI-Flash; AHB2 is extended to AHB Master [1-6] for users to design AHB peripherals. APB bus includes APB1 and APB2, APB bus loads UART0, UART1, Timer0, Timer1, Watch Dog, RTC, DualTimer, TRNG, I2C, SPI, SD-Card;
Start Page
Design Summary
IP Core Generator
Message
(0) (0) (0)
Console
%
Search for anything
ENG
10:34
20/05/2021

GoWin MCU Designer



Keil uVision



Free S/W downloads links

License request Gowin EDA and GMD https://www.gowinsemi.com/en/support/license/
Gowin EDA tool download https://www.gowinsemi.com/en/support/download_eda/
Free Keil MDK lite restricted to 32Kbyte code size - https://www2.keil.com/mdk5/install
GoWin MCU Designer (GMD) https://www.gowinsemi.com/en/support/database/1331/

Gowin Empu - FPGA and M1/M3 ref designs https://www.gowinsemi.com/en/support/database/569/
V1.3 – hard core on GoWin eval boards
V1.6.2 – soft core on GoWin eval boards

Typical applications

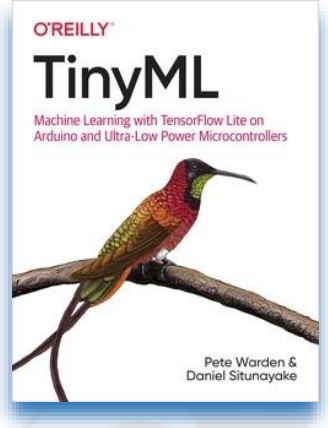
IOT – Multiple sensor input aggregation, display driving, etc, etc

Microcontroller replacement – customise the peripherals required

AI – next section

GoAI 2.0 Design Flow

Aligns with TinyML Commonly Adopted ML Design Flow



1) Training Framework
   - Tensorflow / Keras
   - Almost any model can be converted from Caffe to TensorFlow
2) Testing
   - Tensorflow / Keras
3) Optimization
   - Tensorflow Lite / Keras
4) GoAI 2.0 Assembler
   - FPGA Bitstream
   - Model Coefficients
   - MCU Firmware
5) Deployment
   - GOWIN Programmer

GoAI 2.0 Hardware Accelerator

1) GW1NSR4P

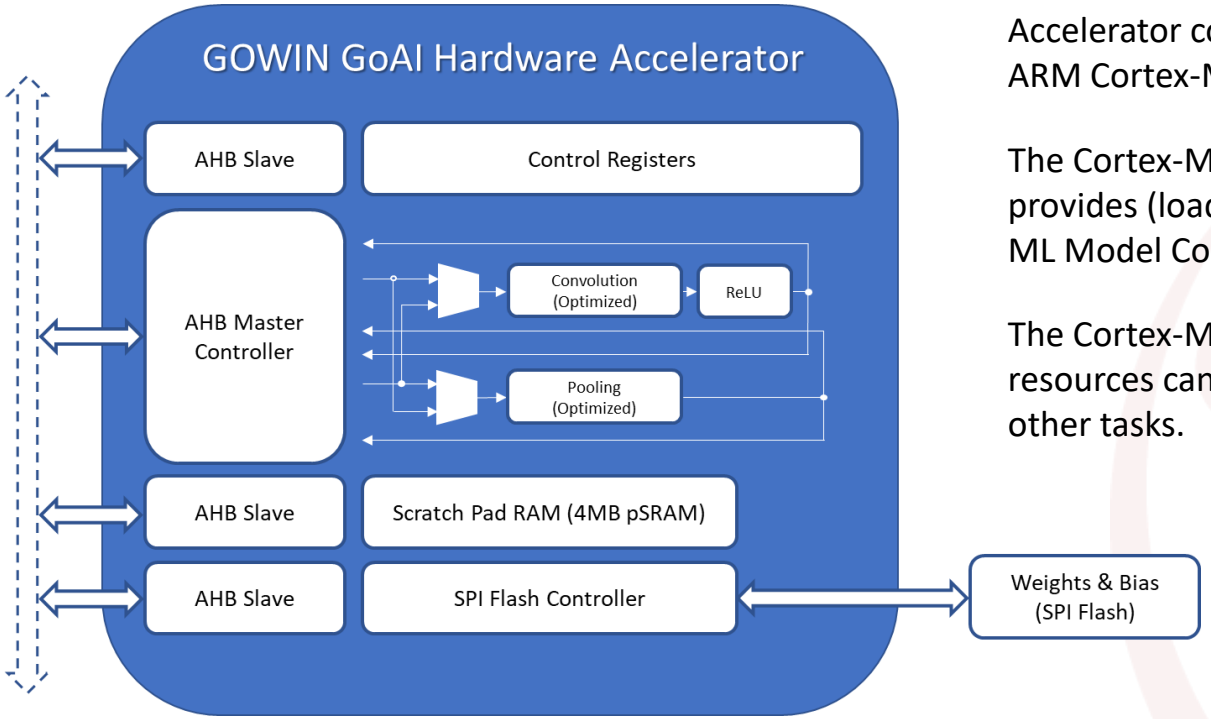
- Supports 1x Accelerator
- Low-Cost & Low-Power
- Multiple GW1NSR4P devices can be used to implement different ML models.

2) GW2AR18P

- Supports 2x Accelerators
- QN88 package device has two separate pSRAM partitions

3) GW2A55P

- Supports Multiple Accelerators
- Utilizes B-SRAM rather than pSRAM for Scratch Pad Memory.
- The number of Accelerators depends on the model.



Accelerator controlled by the ARM Cortex-M processor.

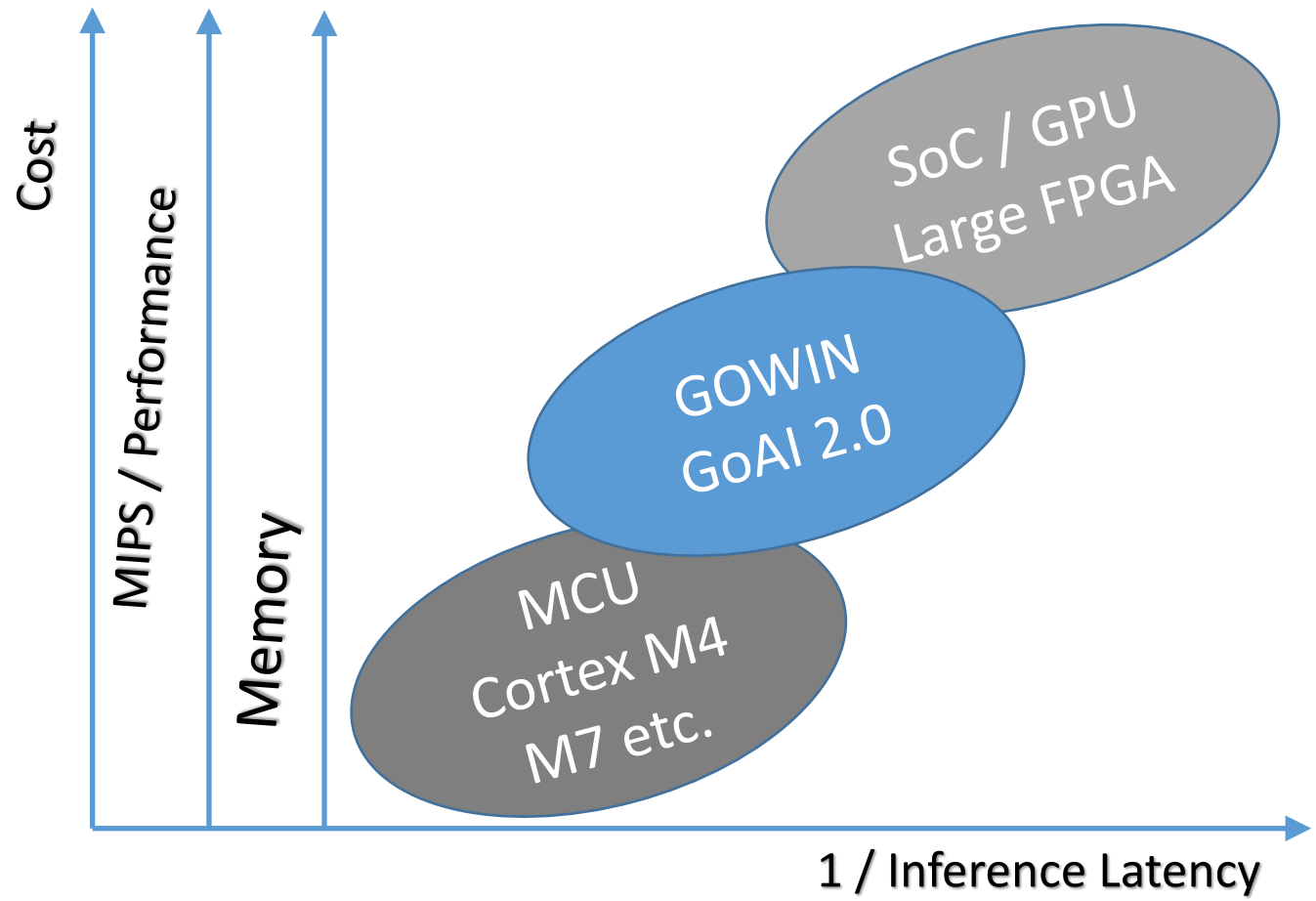
The Cortex-M processor provides (loads) the Accelerator ML Model Coefficients.

The Cortex-M processor resources can also be used for other tasks.

Multi Model Use Cases

- Different Field-of-Views from the same camera.
- Downscaled images to detect objects further away.
- Using two types of sensors like microphone and camera.

GoAI 2.0 Market Positioning



GOWIN GoAI 2.0

Provides advantages over existing MCU ML platforms.

- Higher performance
- Lower Power
- Flexible Interfacing & Buffering
- Data Pre-Processing

GoAI Successes

Person Classification

- Virtual Reality / Augmented Reality Headset Application

Car Classification

- Entrance Monitoring

Person Classification

- Regional & Variable Depth Field-of-View for Security/Surveillance

Digit Classification

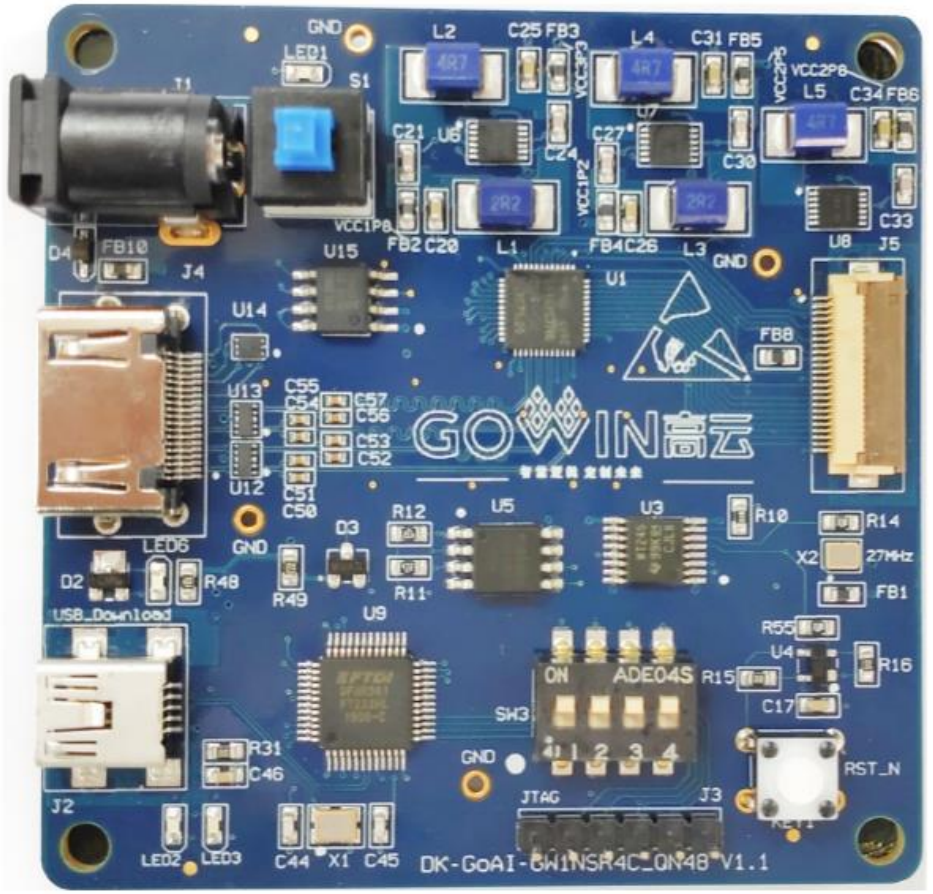
- Utility Meters (Design in Progress)

DK-GOAI-GW1NSR4C Eval Board

GOWIN FPGA-SoC GW1NSR-4C-QN48P

- Embedded ARM Cortex-M3
- FPGA 4.6K LUTs
- Block-SRAM 180Kbit
- User Flash 256Kbit
- Memory 8MB pSRAM
- QFN48 Package 6x6mm

- Camera OV2640 1600x1200
- 2x Microphone I2S SPH0645
- IMU Accelerometer LSM9DS1
- HDMI TX
- External 8MB SPI FLASH
- USB Programmer
- PCB Size: 4cm x 6.5cm



Keil ULINK2 In-Circuit Emulator

Feature	ULINK*pro*	ULINK*proD*	ULINK*plus*	ULINK2
Debug & Trace				
Serial Wire Debug (SWD)	✓	✓	✓	✓
Data Trace (ITM)	✓	✓	✓	✓
Data & Event Trace (SWO)	100 Mbit/s	100 Mbit/s	50 Mbit/s	1 Mbit/s
Instruction Trace (ETM)	800 Mbit/s			
Supported Devices				
ARM7/9	✓	✓		✓
Arm Cortex-M series	✓	✓	✓	✓
XC800/µPSD/XC166/LPC950				✓
Energy measurement & Test I/O			✓	
Electric isolation (1 kV)	optional	optional	integrated	
I/O Voltage Range	1.2 V -3.3 V	1.2 V-3.3 V	1.2 V-5.5 V	2.7 V-5.5 V
Target Connector				
10-pin (0.05”), 20-pin (0.10”)	✓	✓	✓	✓
20-pin (0.05”)	✓	✓		
Connects to				
Keil MDK	✓	✓	✓	✓
Keil PK51, PK166				✓
Arm DS-5	✓	✓	✓	
Order-Code	ULINKPRO	ULINKPRO-D	ULINKPLUS	ULINK2

REDTREE SOLUTIONS

	J-Link	J-Link Pro	J-Trace Cortex-M
USB	yes	yes	yes
Ethernet	no	yes	no
Supported Cores	Cortex-M ARM7, ARM9	Cortex-M ARM7, ARM9	Cortex-M ARM7, ARM9 - no tracing
JTAG	yes	yes	yes
SWD	yes	yes	yes
SWO	yes	yes	yes
ETM Trace	no	no	yes